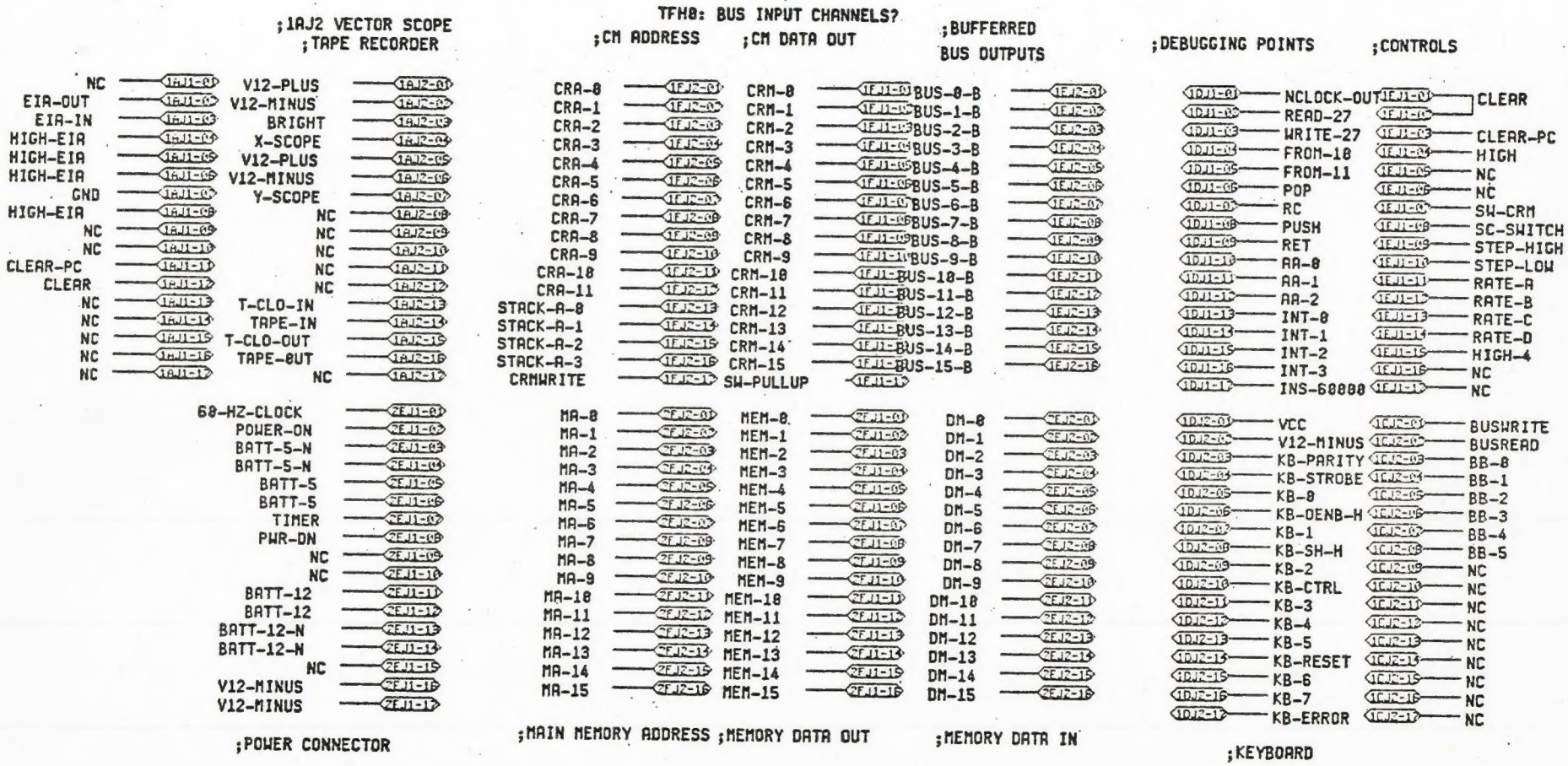
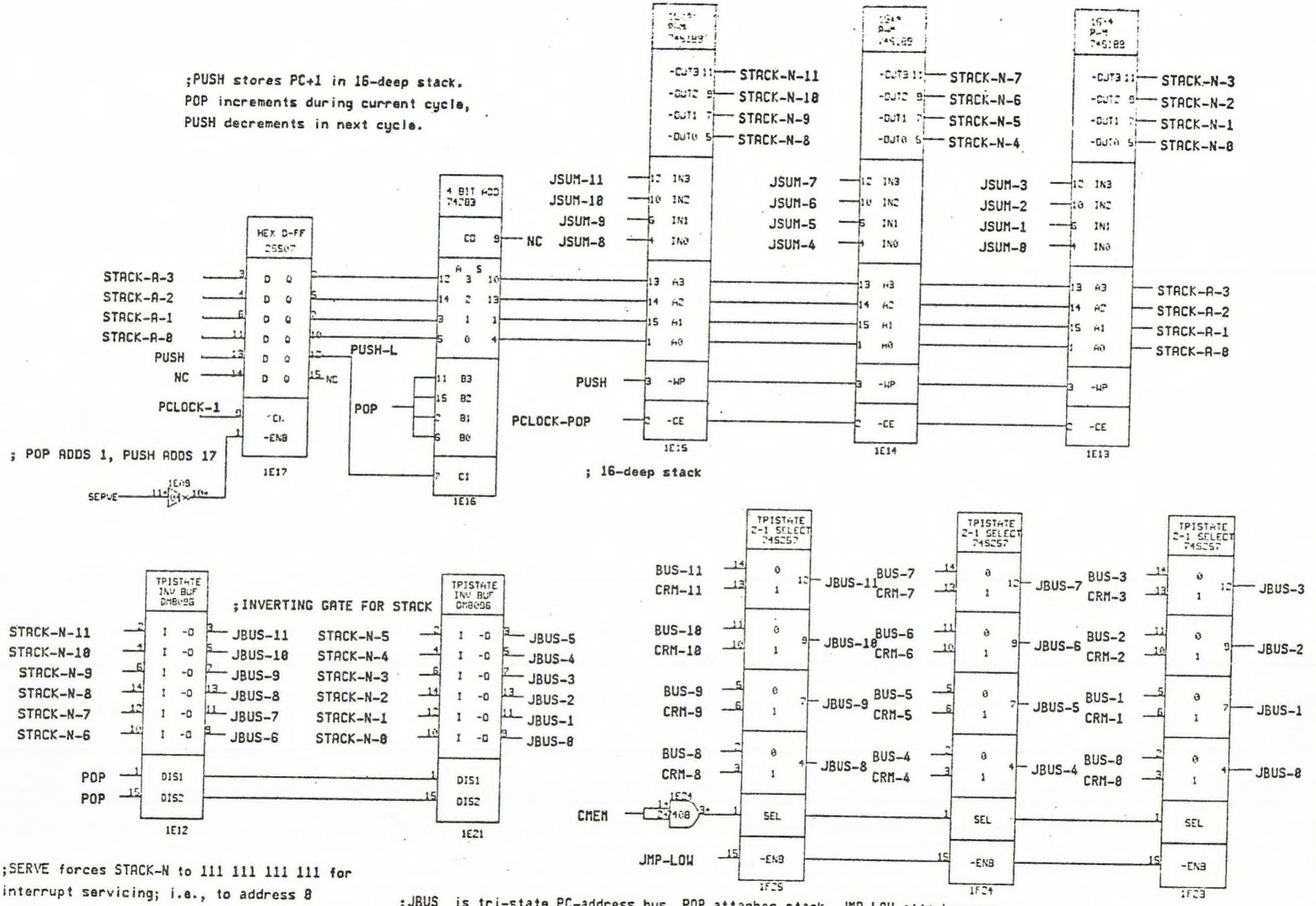
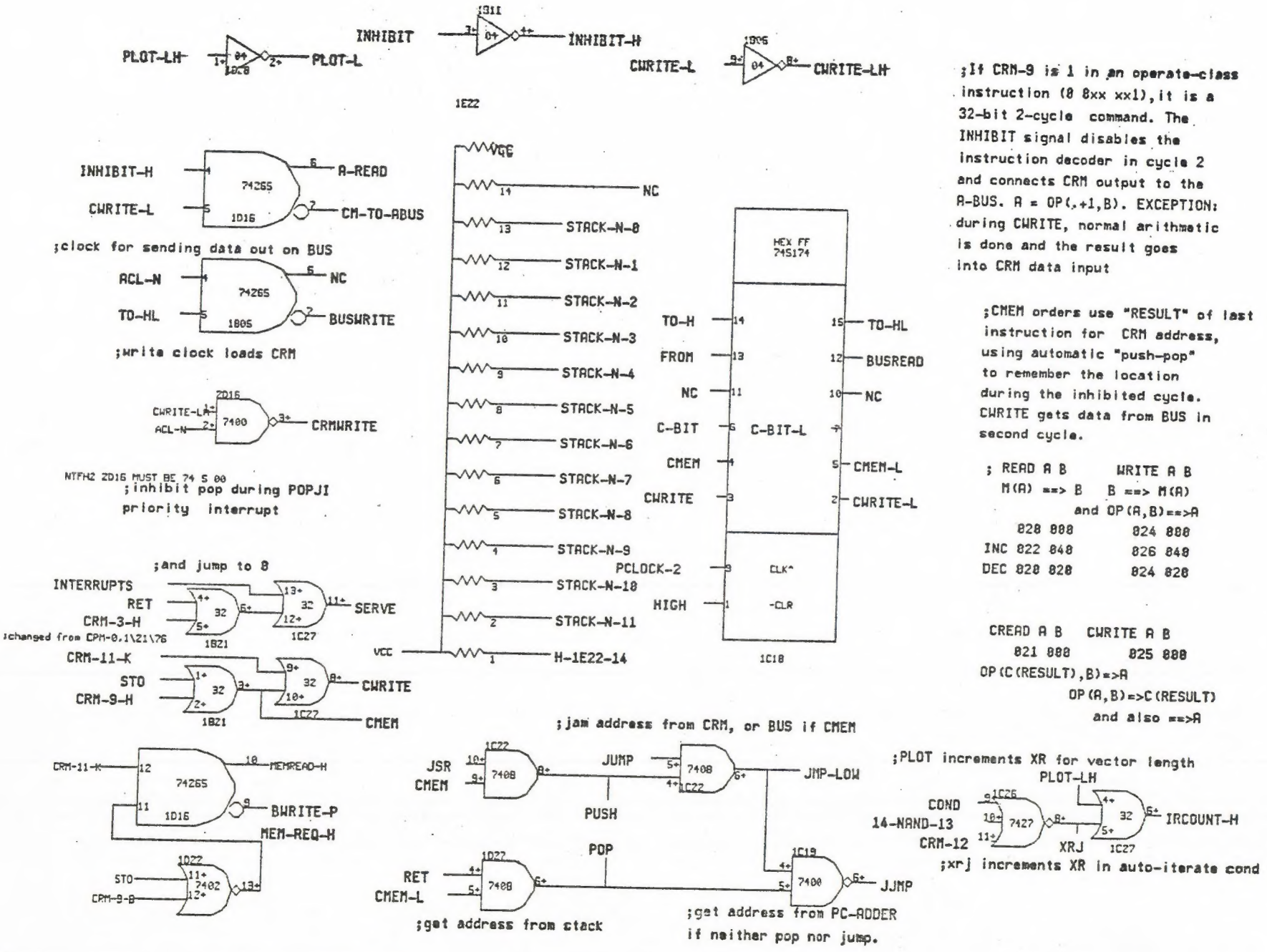
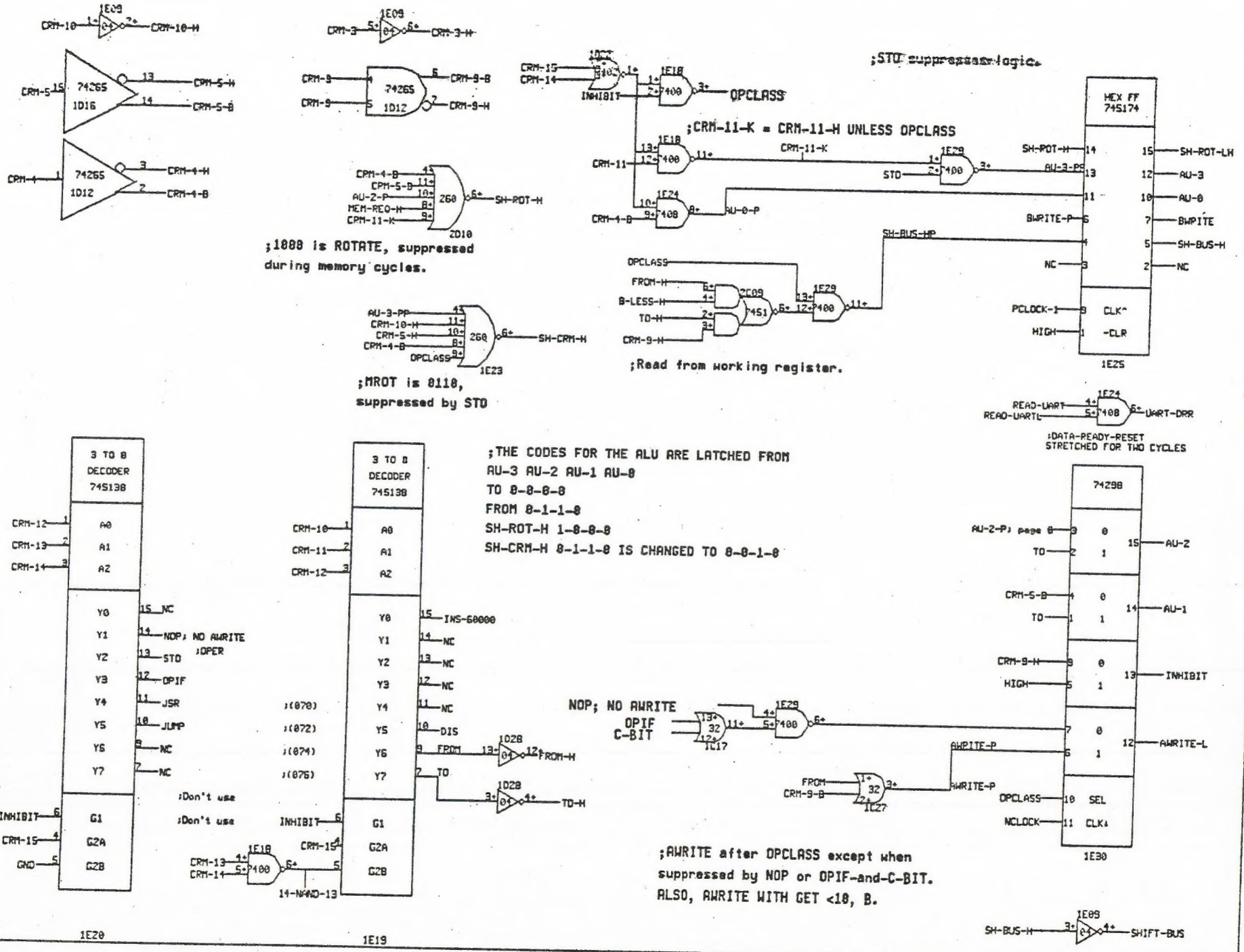

;1AJ2 VECTOR SCOPE
;TAPE RECORDER
NC
EIA-OUT
EIA-IN
HIGH-EIA
HIGH-EIA
HIGH-EIA
GND
HIGH-EIA
NC
NC
CLEAR-PC
CLEAR
NC
NC
NC
NC
V12-PLUS
V12-MINUS
BRIGHT
X-SCOPE
V12-PLUS
V12-MINUS
Y-SCOPE
NC
NC
NC
NC
NC
T-CLO-IN
TAPE-IN
T-CLO-OUT
TAPE-OUT
NC
68-HZ-CLOCK
POWER-ON
BATT-5-N
BATT-5-N
BATT-5
BATT-5
TIMER
PWR-DN
NC
NC
BATT-12
BATT-12
BATT-12-N
BATT-12-N
NC
V12-MINUS
V12-MINUS
;POWER CONNECTOR
TFH8: BUS INPUT CHANNELS?
;CM ADDRESS
;CM DATA OUT
;BUFFERRED
BUS OUTPUTS
CRA-0
CRA-1
CRA-2
CRA-3
CRA-4
CRA-5
CRA-6
CRA-7
CRA-8
CRA-9
CRA-10
CRA-11
STACK-A-0
STACK-A-1
STACK-A-2
STACK-A-3
CRMWRITE
CRM-0
CRM-1
CRM-2
CRM-3
CRM-4
CRM-5
CRM-6
CRM-7
CRM-8
CRM-9
CRM-10
CRM-11
CRM-12
CRM-13
CRM-14
CRM-15
SW-PULLUP
BUS-0-B
BUS-1-B
BUS-2-B
BUS-3-B
BUS-4-B
BUS-5-B
BUS-6-B
BUS-7-B
BUS-8-B
BUS-9-B
BUS-10-B
BUS-11-B
BUS-12-B
BUS-13-B
BUS-14-B
BUS-15-B
;DEBUGGING POINTS
;CONTROLS
NCLOCK-OUT
READ-27
WRITE-27
FROM-10
FROM-11
POP
RC
PUSH
RET
AA-0
AA-1
AA-2
INT-0
INT-1
INT-2
INT-3
INS-60000
CLEAR
CLEAR-PC
HIGH
NC
NC
SW-CRM
SC-SWITCH
STEP-HIGH
STEP-LOW
RATE-A
RATE-B
RATE-C
RATE-D
HIGH-4
NC
NC
MA-0
MA-1
MA-2
MA-3
MA-4
MA-5
MA-6
MA-7
MA-8
MA-9
MA-10
MA-11
MA-12
MA-13
MA-14
MA-15
MEM-0
MEM-1
MEM-2
MEM-3
MEM-4
MEM-5
MEM-6
MEM-7
MEM-8
MEM-9
MEM-10
MEM-11
MEM-12
MEM-13
MEM-14
MEM-15
DM-0
DM-1
DM-2
DM-3
DM-4
DM-5
DM-6
DM-7
DM-8
DM-9
DM-10
DM-11
DM-12
DM-13
DM-14
DM-15
;MAIN MEMORY ADDRESS
;MEMORY DATA OUT
;MEMORY DATA IN
VCC
V12-MINUS
KB-PARITY
KB-STROBE
KB-0
KB-DENB-H
KB-1
KB-SH-H
KB-2
KB-CTRL
KB-3
KB-4
KB-5
KB-RESET
KB-6
KB-7
KB-ERROR
BUSWRITE
BUSREAD
BB-0
BB-1
BB-2
BB-3
BB-4
BB-5
NC
NC
NC
NC
NC
NC
NC
NC
;KEYBOARD

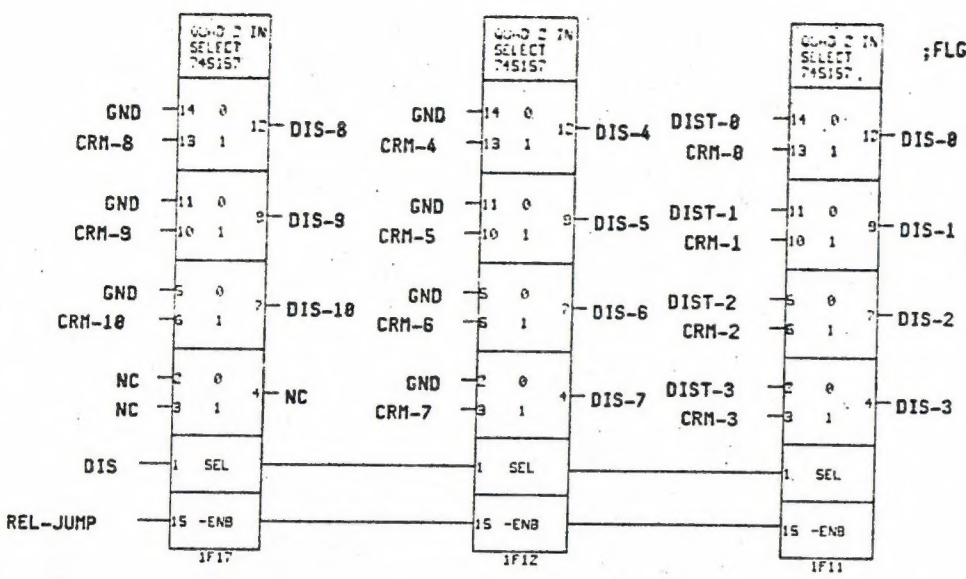


STACK TO PC GATE	STACK	05-APR-76 14:20	HQM: NTFH1

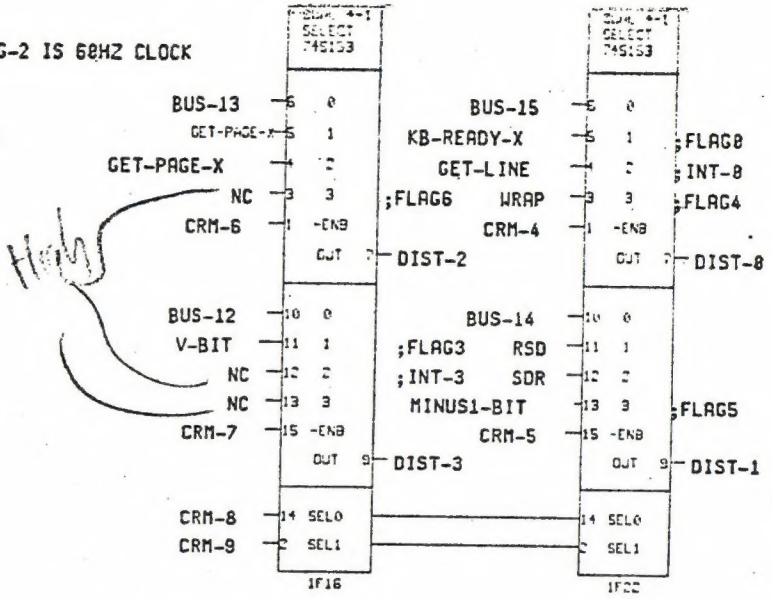

PLOT-LH
PLOT-L
INHIBIT
INHIBIT-H
CWRITE-L
CWRITE-LH
1E22
INHIBIT-H
CWRITE-L
A-READ
CM-TO-ABUS
74265
1D16
;clock for sending data out on BUS
ACL-N
TO-HL
NC
BUSWRITE
1B05
;write clock loads CRM
CWRITE-LH
ACL-N
7400
CRMWRITE
2D16
NTFH2 2D16 MUST BE 74 S 00
;inhibit pop during POPJI
priority interrupt
;and jump to 8
INTERRUPTS
RET
CRM-3-H
;changed from CPM-0.1\21\76
SERVE
1B21
1C27
CRM-11-K
STO
CRM-9-H
CWRITE
CMEM
VCC
NC
STACK-N-0
STACK-N-1
STACK-N-2
STACK-N-3
STACK-N-4
STACK-N-5
STACK-N-6
STACK-N-7
STACK-N-8
STACK-N-9
STACK-N-10
STACK-N-11
H-1E22-14
HEX FF
74S174
TO-H
FROM
NC
C-BIT
CMEM
CWRITE
PCLOCK-2
HIGH
C-BIT-L
CLK^
-CLR
TO-HL
BUSREAD
CMEM-L
CWRITE-L
1C18
;If CRM-9 is 1 in an operate-class instruction (0 8xx xx1), it is a 32-bit 2-cycle command. The INHIBIT signal disables the instruction decoder in cycle 2 and connects CRM output to the A-BUS. A = OP(,+1,B). EXCEPTION: during CWRITE, normal arithmetic is done and the result goes into CRM data input
;CMEM orders use "RESULT" of last instruction for CRM address, using automatic "push-pop" to remember the location during the inhibited cycle. CWRITE gets data from BUS in second cycle.
; READ A B
M(A) ==> B
WRITE A B
B ==> M(A)
and OP(A,B)==>A
828 888
824 888
INC 822 848
826 848
DEC 828 828
824 828
CREAD A B
821 888
CWRITE A B
825 888
OP(C(RESULT),B)=>A
OP(A,B)=>C(RESULT)
and also ==>A
CRM-11-K
MEMREAD-H
BWRITE-P
MEM-REQ-H
1D22
STO
CRM-9-B
;jam address from CRM, or BUS if CMEM
JSR
CMEM
JUMP
PUSH
JMP-LOW
RET
CMEM-L
POP
JJMP
;get address from stack
;get address from PC-ADDER if neither pop nor jump.
;PLOT increments XR for vector length
PLOT-LH
COND
14-NAND-13
CRM-12
IRCOUNT-H
XRJ
7427
;xrj increments XR in auto-iterate cond



INSTRUCTION DECODER	MINSKY 2500	29-FEB-76 13:07	HQM: NTFH3



;FLG-2 IS 60HZ CLOCK



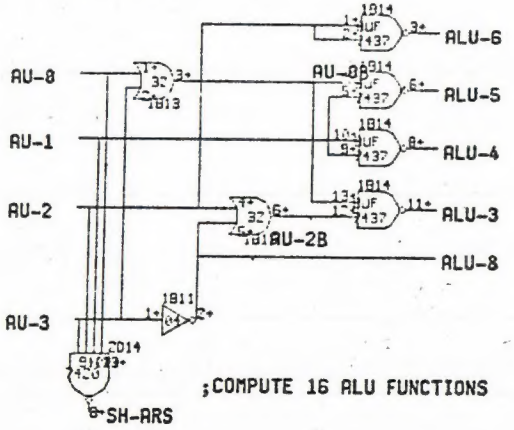
;MINUS1-BIT is low if BUS=177777

;RSD is UART data-out-ready

;SDR is UART-data-in-ready

;DISPATCH SELECTORS SHOULD BE S CHIPS
;DIS COMMAND SEL(2) MASK(4) 0000 MASK INVERTED

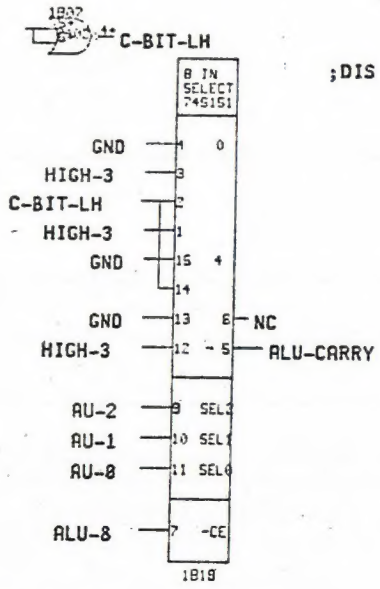
;7437'S REQUIRED TO DRIVE LARGE ALU LOAD



;COMPUTE 16 ALU FUNCTIONS

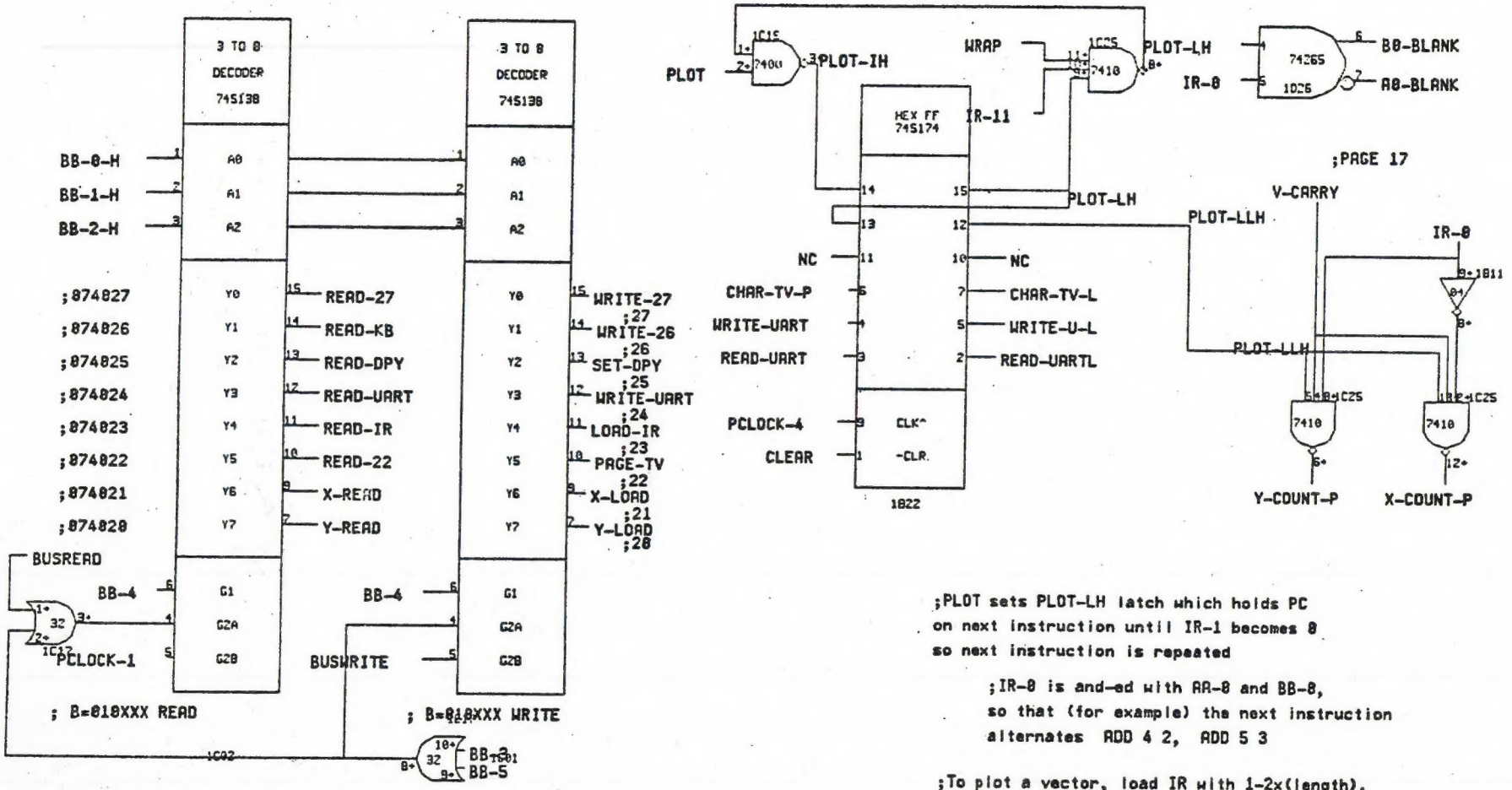
; OP IS 1111

C-BIT-L



;pin 6 inverts, diagram wrong!

; LOGIC	ARITHMETIC	
0000 A	4000	ROTATE
0020 AB'	4020	A - 1
0040 AB	4040	ADC
0060 NOR	4060	A+B
2000 OR	6000	A - B
2020 XOR	6020	SBC
2040 MROT	6040	A + 1
2060 ?	6060	ARS



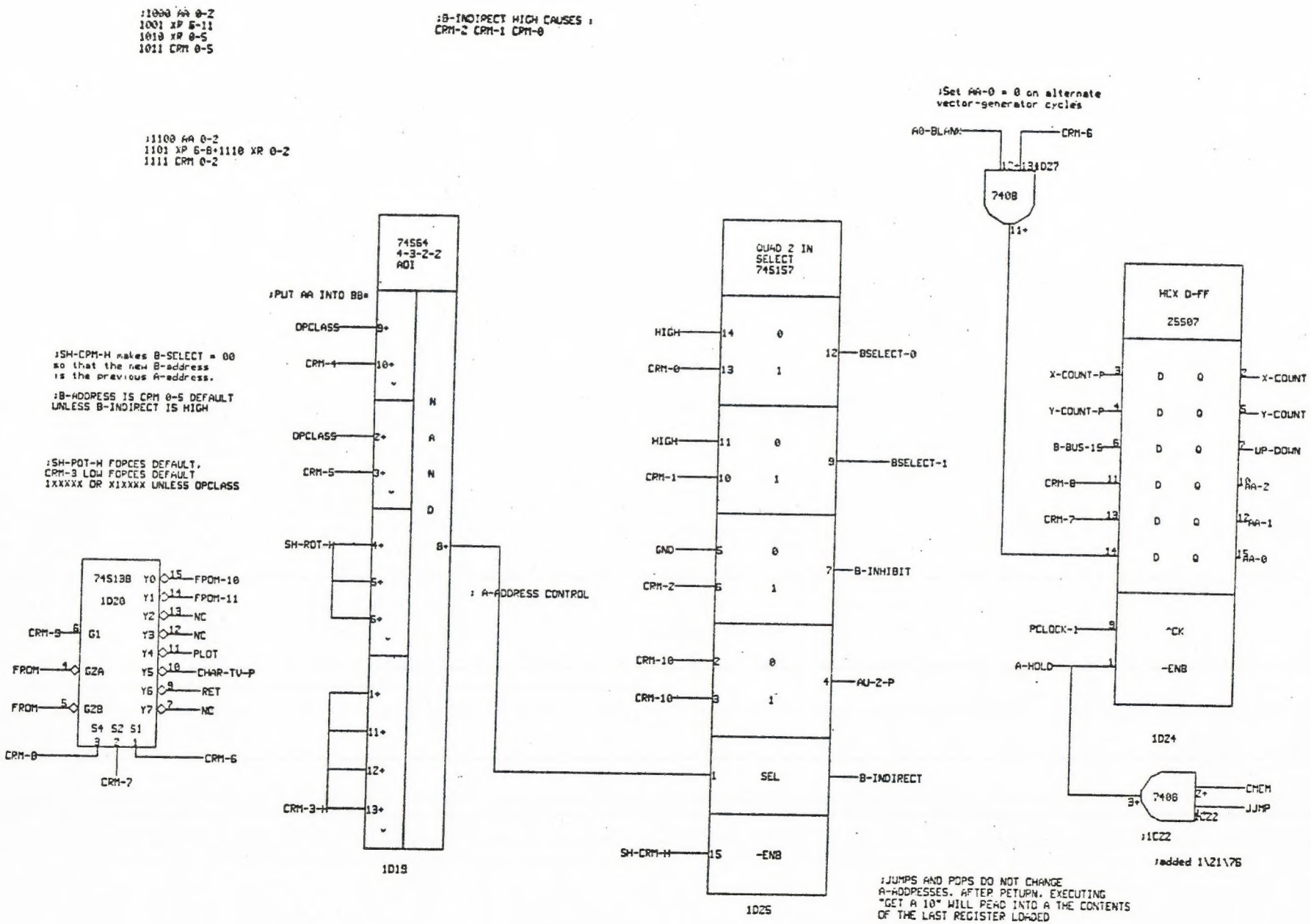
;NOTE: WRITE-UART is latched to stretch 220ns pulse

;NOTE BUSWRITE is an 88 ns pulse

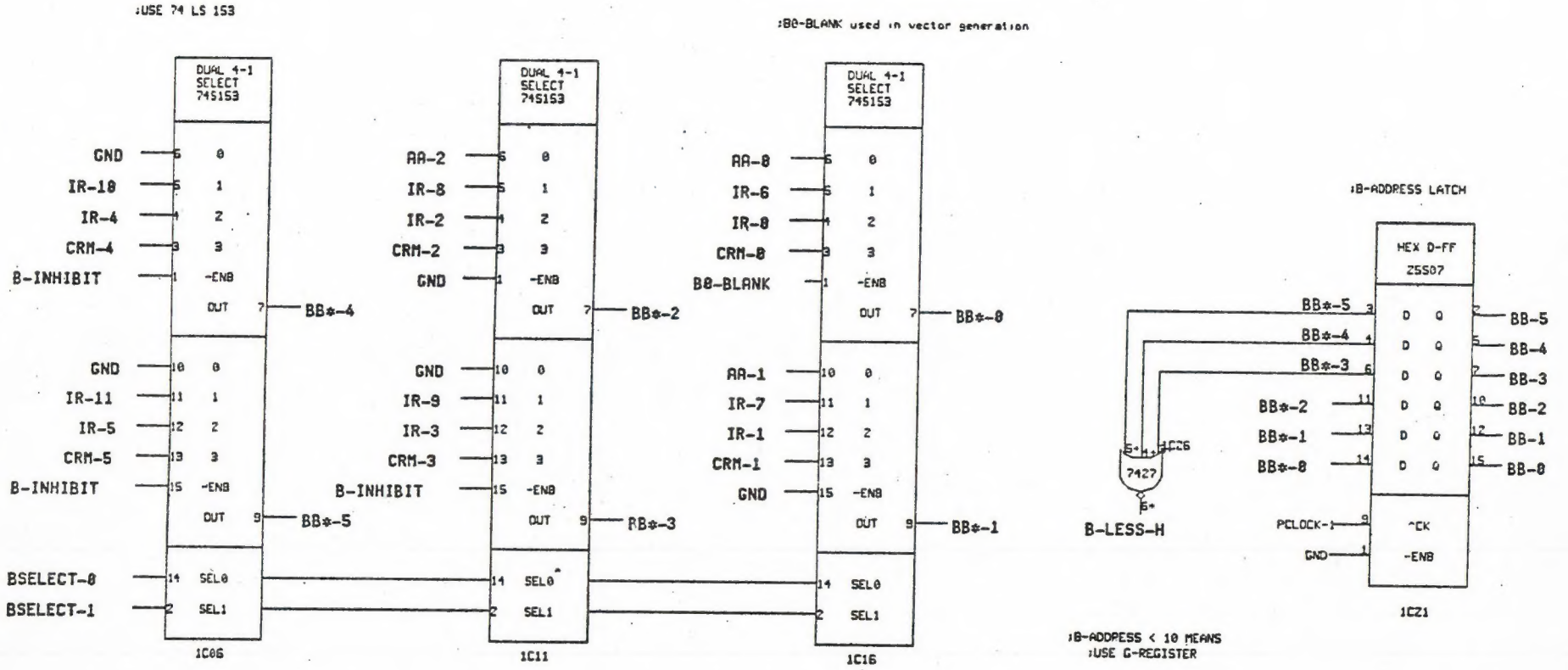
;PLOT sets PLOT-LH latch which holds PC on next instruction until IR-1 becomes 0 so next instruction is repeated

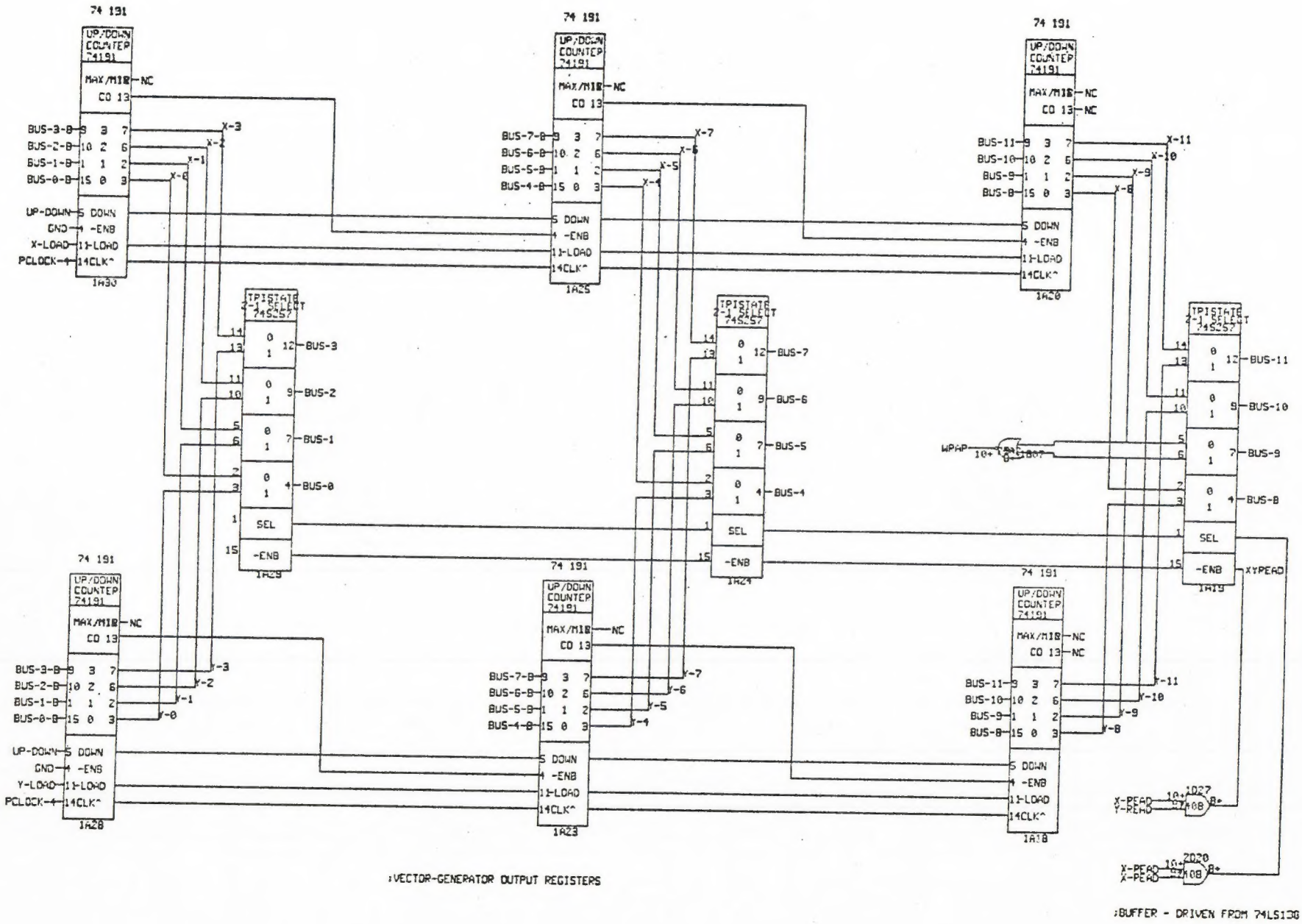
;IR-0 is and-ed with AR-0 and BB-0, so that (for example) the next instruction alternates ADD 4 2, ADD 5 3

;To plot a vector, load IR with 1-2x(length). When an ADD overflows, the X or Y counter selected by IR-0 is incremented or decremented according to the sign of the B-addend.

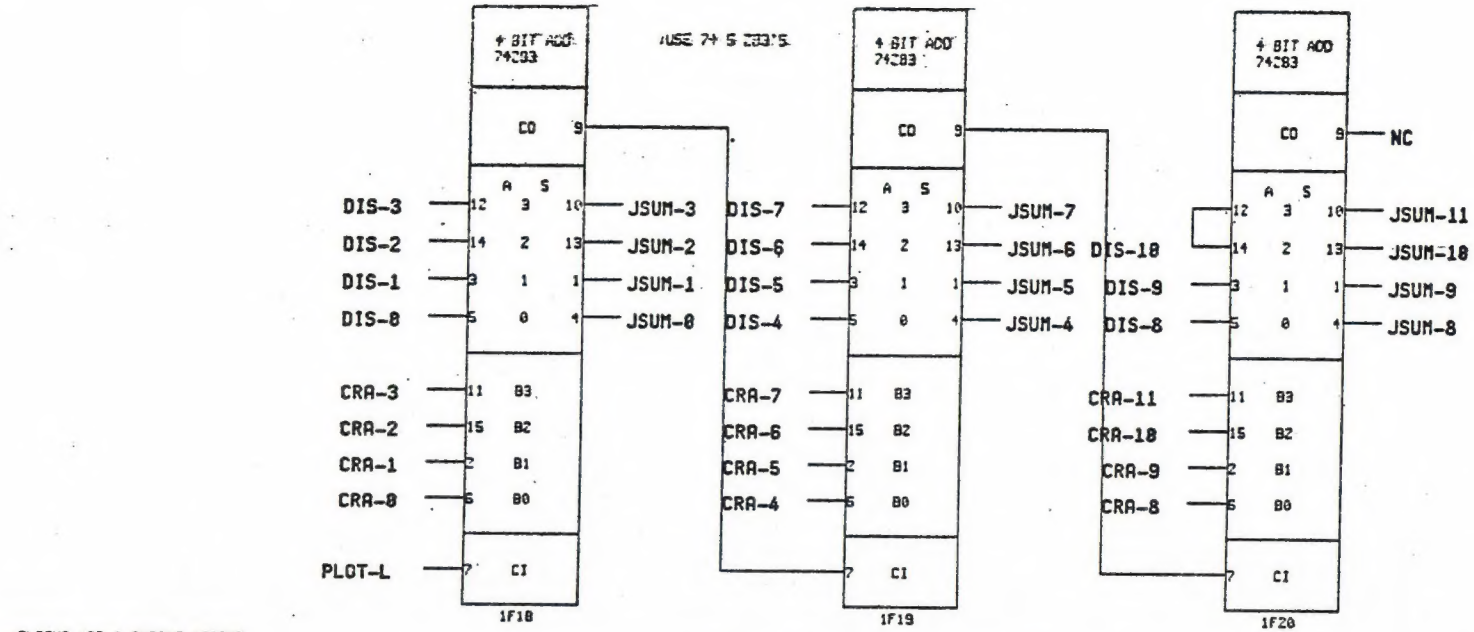


ADDRESS CONTROL	MINSKY 2500	29-FEB-76 14:26	HQM: NTFH6


;USE 74 LS 153
;B0-BLANK used in vector generation
DUAL 4-1 SELECT 74S153
GND
IR-10
IR-4
CRM-4
B-INHIBIT
BB*-4
GND
IR-11
IR-5
CRM-5
B-INHIBIT
BB*-5
BSELECT-0
BSELECT-1
1C06
AA-2
IR-8
IR-2
CRM-2
GND
BB*-2
GND
IR-9
IR-3
CRM-3
B-INHIBIT
BB*-3
1C11
AA-0
IR-6
IR-0
CRM-0
B0-BLANK
BB*-0
AA-1
IR-7
IR-1
CRM-1
GND
BB*-1
1C16
;B-ADDRESS LATCH
HEX D-FF
2S507
BB*-5
BB*-4
BB*-3
BB*-2
BB*-1
BB*-0
BB-5
BB-4
BB-3
BB-2
BB-1
BB-0
7427
1C26
B-LESS-H
PCLOCK-1
GND
1CZ1
;B-ADDRESS < 10 MEANS
;USE G-REGISTER
;IF B-ADDRESS IS SELECT FOR B-ADDRESS SOURCE
; 10 AA 0-2. This is forced by SH-CRM-H.
; 11 IR 6-11 or 6-8 if B-inhibit
; 12 IR 0-5 or 0-2 if B-inhibit
;CRM 0-5 DEFAULT



VECTOR GENERATOR	MINSKY 2500	02-APR-76 15:20	HQM: NTFH3

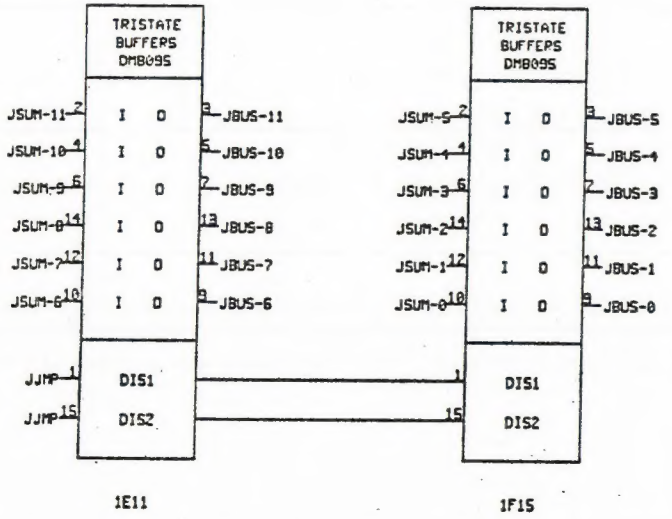


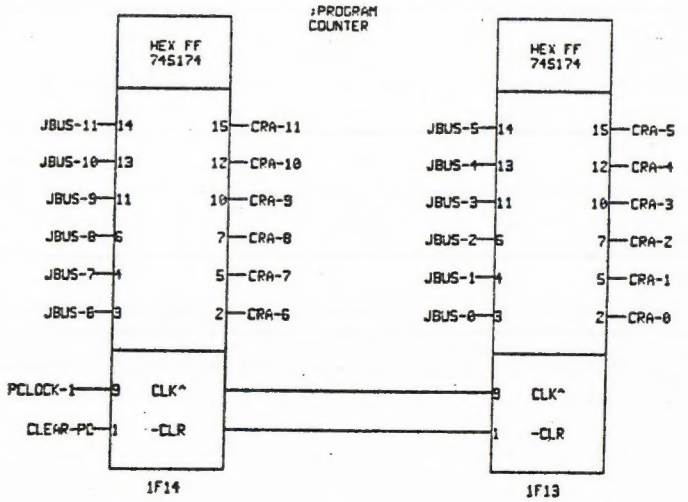
;BLOCKS ADD-1 DURING VECTOR

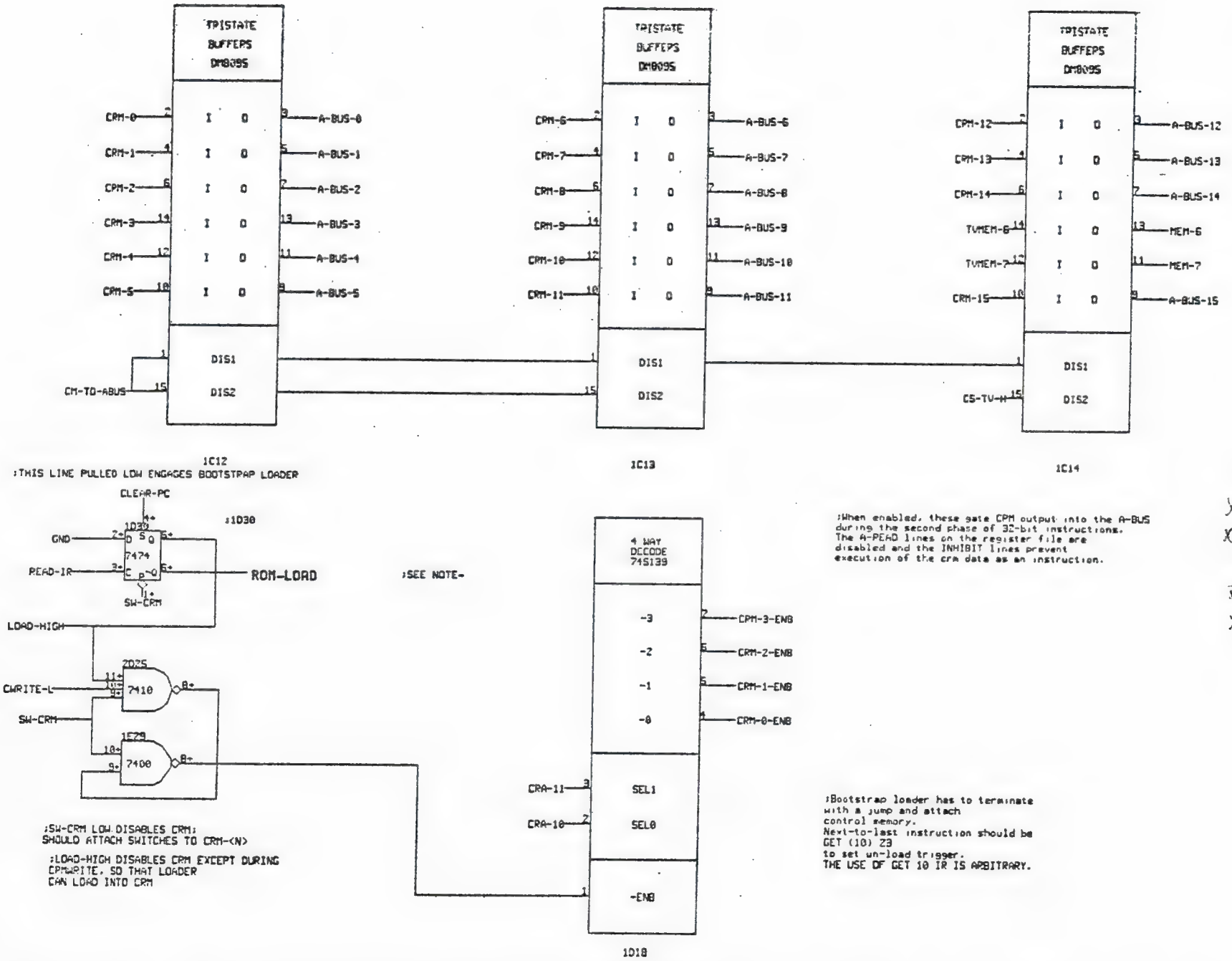
;12 BIT ADDER FOR INCREMENTING AND ADDING DISPATCH OFFSET

;USE 74 S 283'S

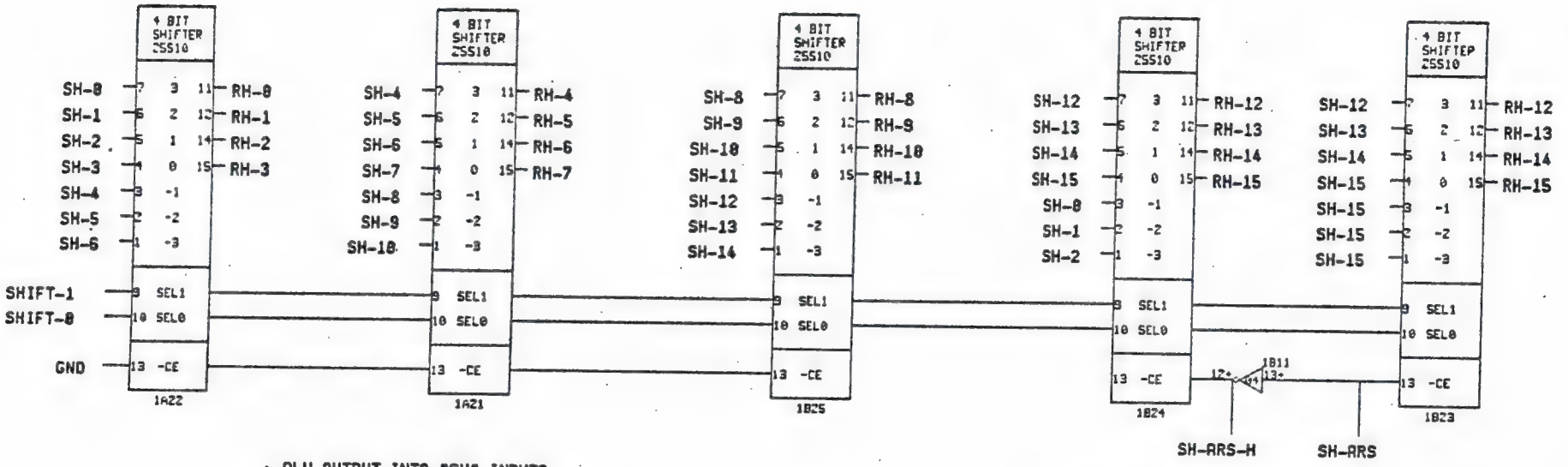
;USE 74 367'S







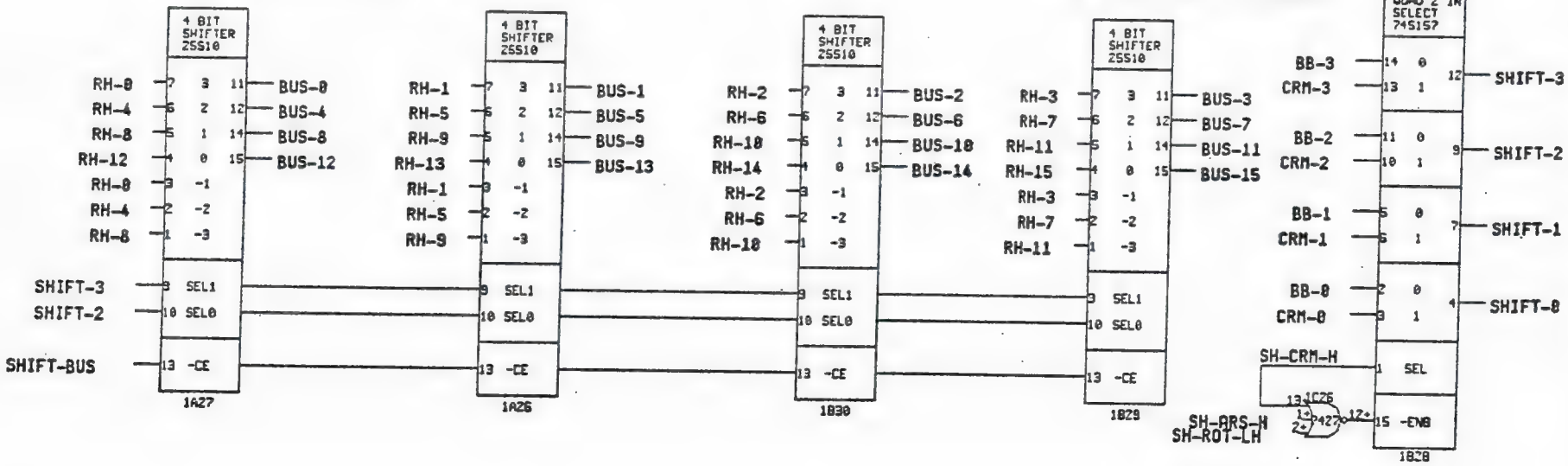
CONTROL MEMORY GATES | 2500 MINSKY | 01-APR-76 12:51 | HQM; NTFH10

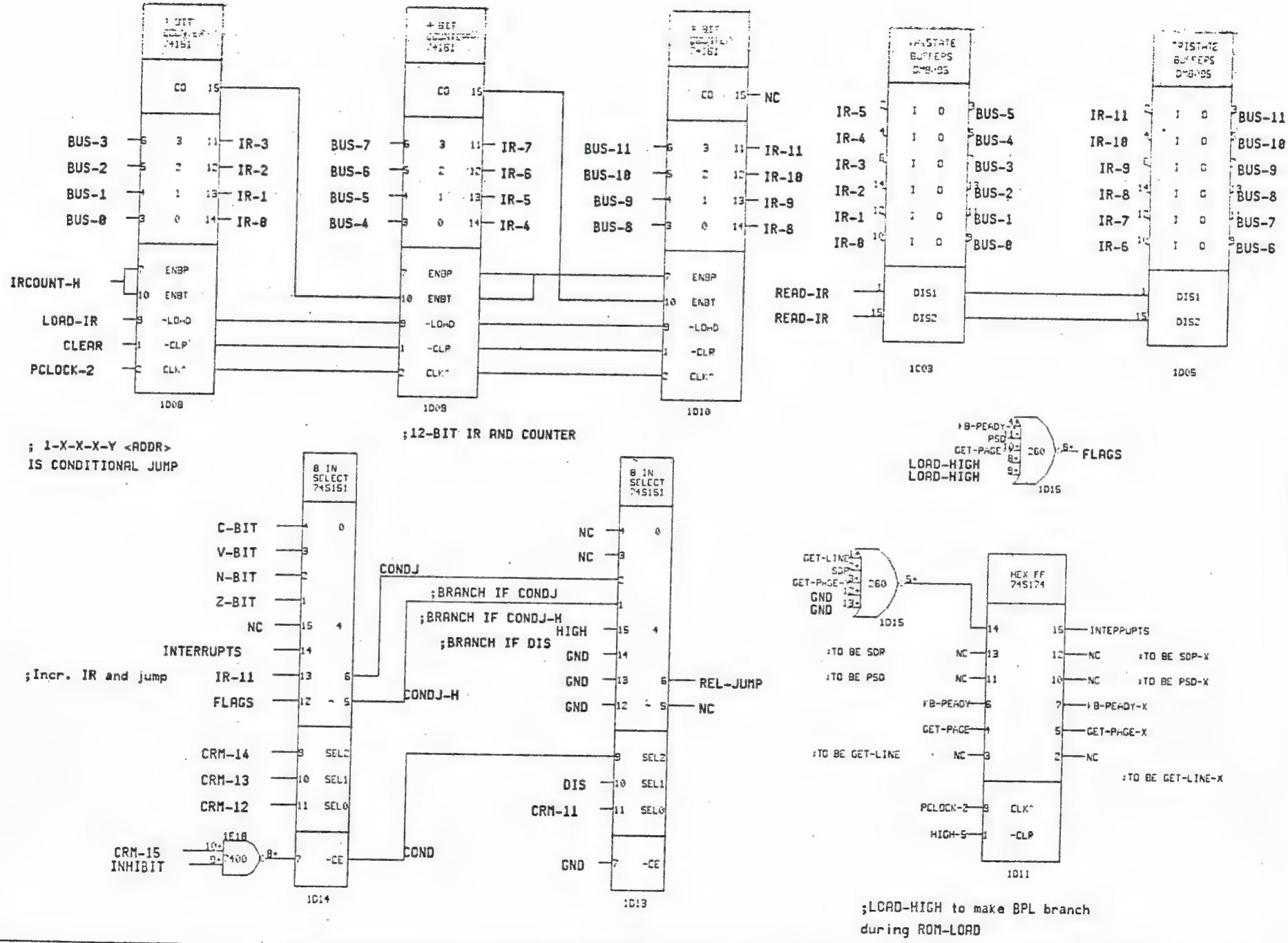


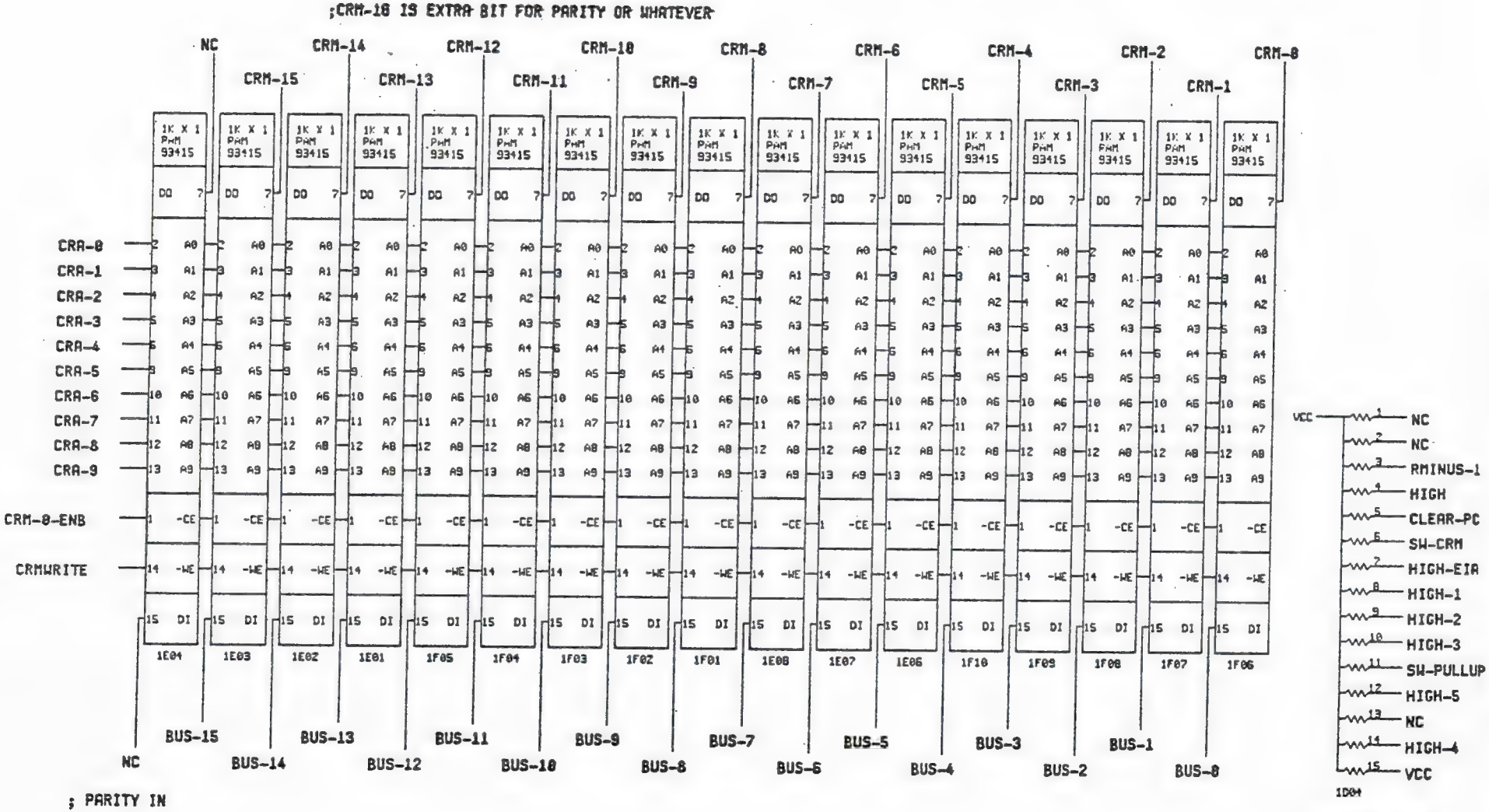
; ALU OUTPUT INTO "SH" INPUTS
; "RH" ARE INTERMEDIATE SHIFT LINES
; SHIFTER OUTPUTS GO TO MAIN BUS

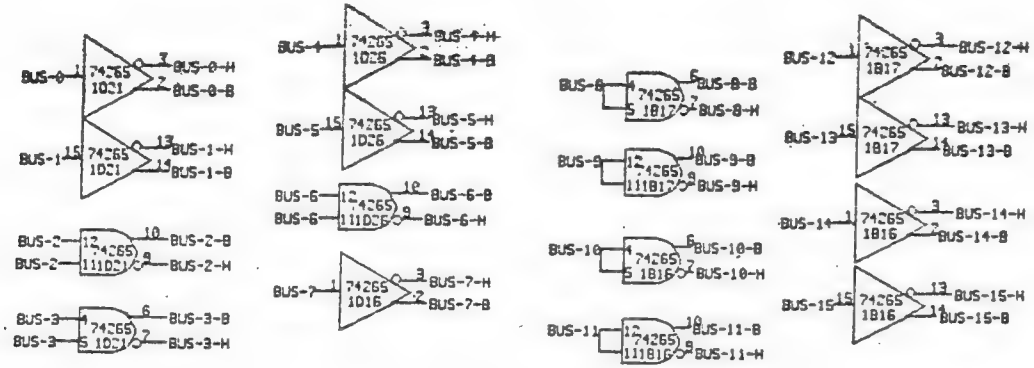
; THREE STEPS OF ARITH RIGHT SHIFT

;SELECT SHIFT SIZE FROM CRM OR B-ADDRESS

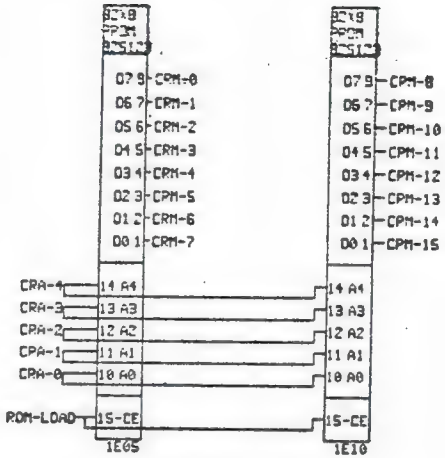



1 BIT
74151
4 BIT
74161
CO
BUS-3
BUS-2
BUS-1
BUS-0
IR-3
IR-2
IR-1
IR-0
BUS-7
BUS-6
BUS-5
BUS-4
IR-7
IR-6
IR-5
IR-4
BUS-11
BUS-10
BUS-9
BUS-8
IR-11
IR-10
IR-9
IR-8
NC
ENBP
ENBT
IRCOUNT-H
-LOAD
LOAD-IR
-CLR
CLEAR
CLK
PCLOCK-2
1D08
1D09
1D10
;12-BIT IR AND COUNTER
; 1-X-X-X-Y <ADDR>
IS CONDITIONAL JUMP
8 IN
SELECT
74S151
C-BIT
V-BIT
N-BIT
Z-BIT
NC
INTERRUPTS
;Incr. IR and jump
IR-11
FLAGS
CONDJ
CONDJ-H
CRM-14
CRM-13
CRM-12
SEL2
SEL1
SEL0
CRM-15
INHIBIT
1E18
7400
-CE
COND
1D14
;BRANCH IF CONDJ
;BRANCH IF CONDJ-H
;BRANCH IF DIS
HIGH
GND
REL-JUMP
DIS
CRM-11
1D13
3-STATE
BUFFERS
DM8-95
TRISTATE
BUFFERS
DM8-95
IR-5
IR-4
IR-3
IR-2
IR-1
IR-0
IR-11
IR-10
IR-9
IR-8
IR-7
IR-6
BUS-5
BUS-4
BUS-3
BUS-2
BUS-1
BUS-0
BUS-11
BUS-10
BUS-9
BUS-8
BUS-7
BUS-6
READ-IR
DIS1
DIS2
1C03
1D05
FB-READY
PSD
GET-PAGE
LOAD-HIGH
LOAD-HIGH
FLAGS
1D15
GET-LINE
SDR
GND
GND
HEX FF
74S174
INTERRUPTS
;TO BE SDR
;TO BE PSD
;TO BE SDR-X
;TO BE PSD-X
FB-READY-X
GET-PAGE-X
;TO BE GET-LINE
;TO BE GET-LINE-X
PCLOCK-2
HIGH-S
CLK
-CLR
1D11
;LOAD-HIGH to make BPL branch
during ROM-LOAD

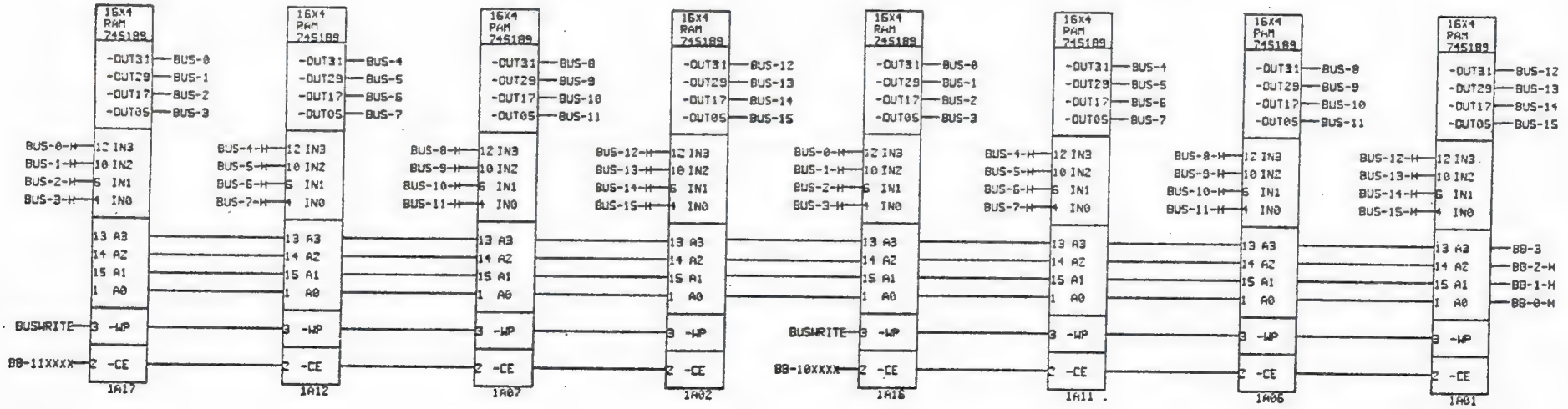

;CRM-16 IS EXTRA BIT FOR PARITY OR WHATEVER
NC
CRM-14
CRM-12
CRM-10
CRM-8
CRM-6
CRM-4
CRM-2
CRM-0
CRM-15
CRM-13
CRM-11
CRM-9
CRM-7
CRM-5
CRM-3
CRM-1
1K X 1 PMM 93415
CRA-0
CRA-1
CRA-2
CRA-3
CRA-4
CRA-5
CRA-6
CRA-7
CRA-8
CRA-9
CRM-0-ENB
CRMWRITE
1E04
1E03
1E02
1E01
1F05
1F04
1F03
1F02
1F01
1E08
1E07
1E06
1F10
1F09
1F08
1F07
1F06
BUS-15
BUS-14
BUS-13
BUS-12
BUS-11
BUS-10
BUS-9
BUS-8
BUS-7
BUS-6
BUS-5
BUS-4
BUS-3
BUS-2
BUS-1
BUS-0
NC
; PARITY IN
VCC
NC
NC
RMINUS-1
HIGH
CLEAR-PC
SW-CRM
HIGH-EIA
HIGH-1
HIGH-2
HIGH-3
SW-PULLUP
HIGH-5
NC
HIGH-4
VCC
1D04
;14-PIN PULLUP
;USE 93425 TRI-STATE RAMS

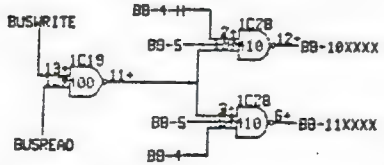


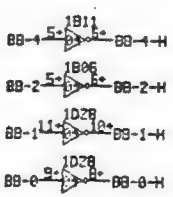
;BUS BUFFERRED FOR GENERAL OUTPUT USE



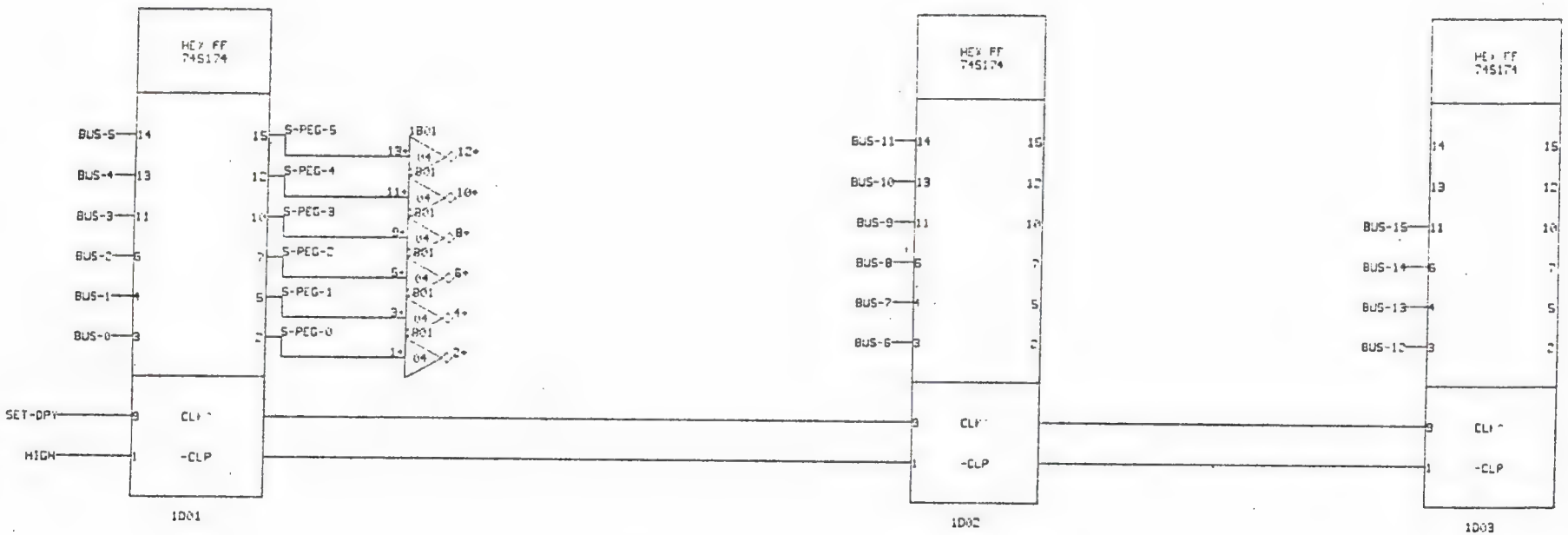
;SOCKETS FOR TWO 32 X 8
ROMS FOR LOADER

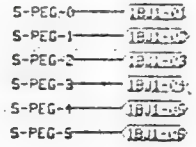






SCRATCHPAD REGISTERS | 29-FEB-76 13:25 | HQM: NTFH14



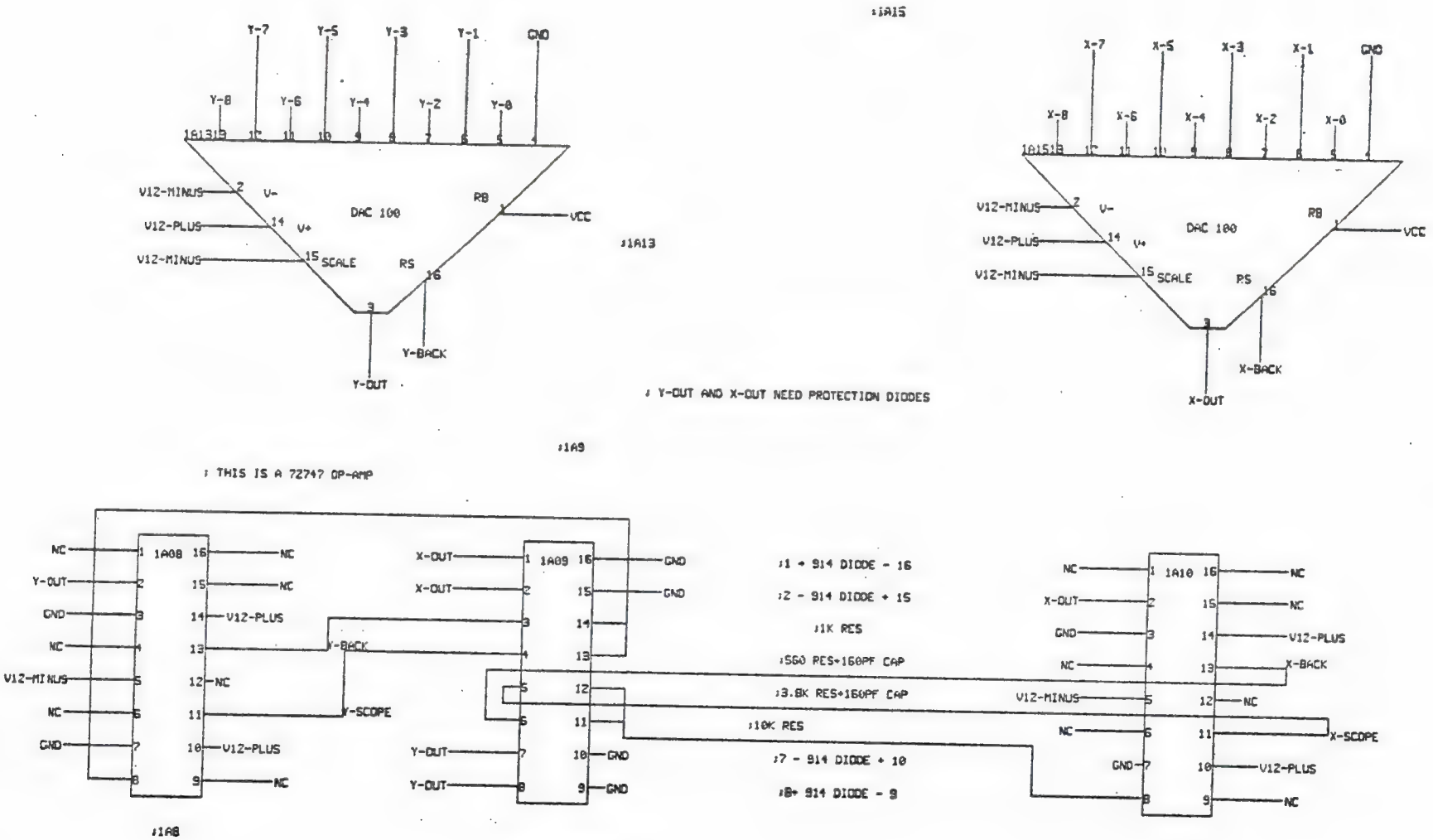


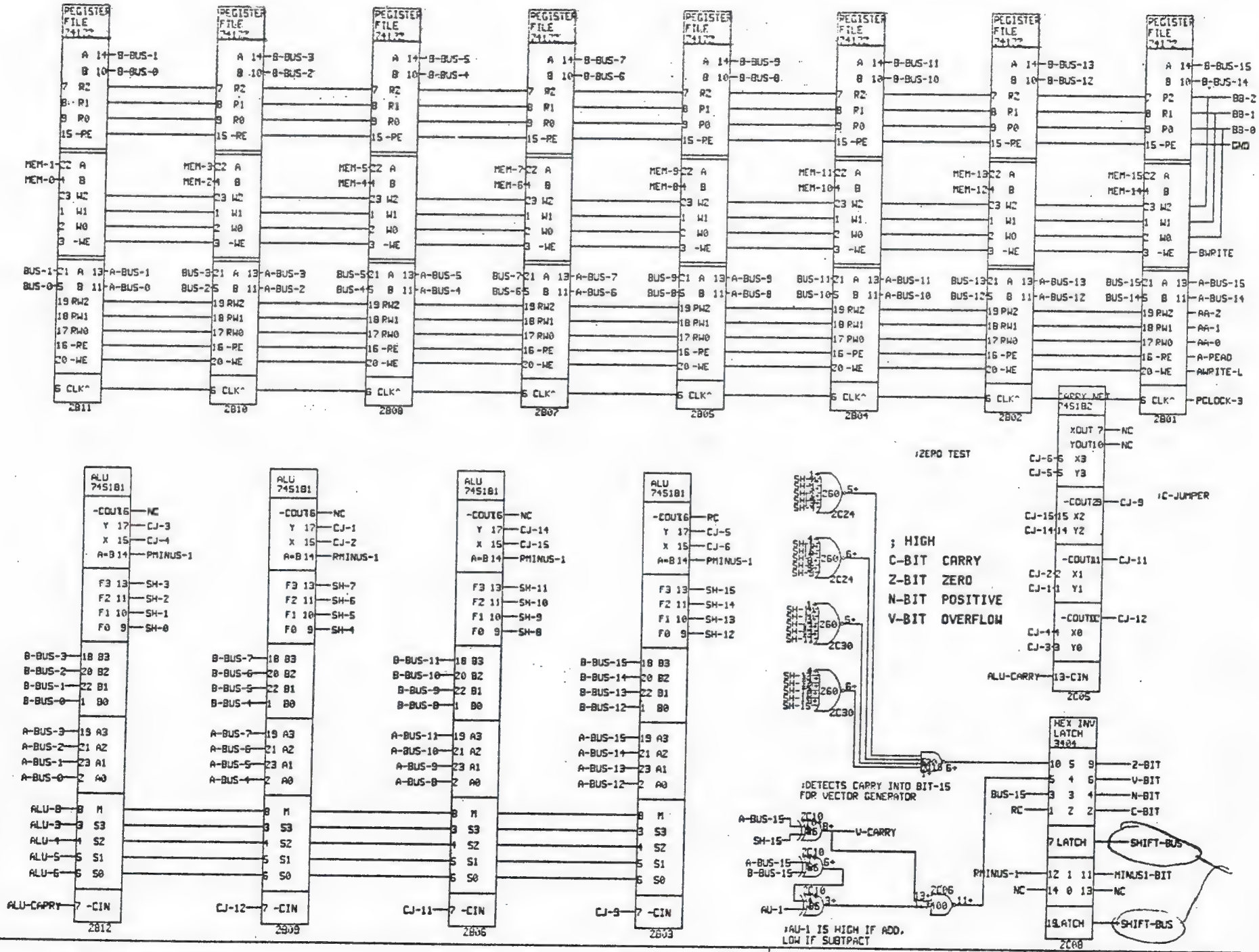
NOTES

TFH ORDER CODE

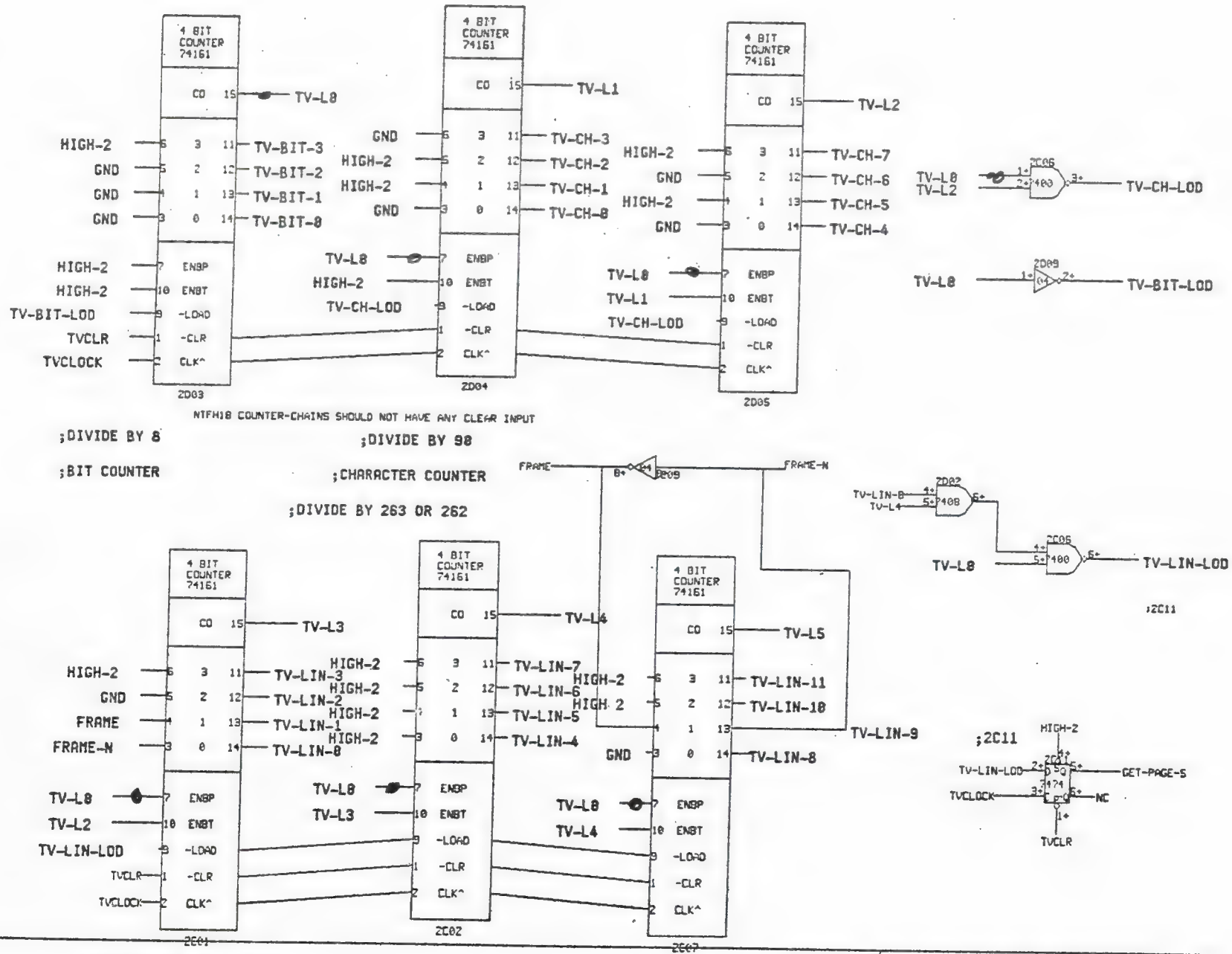
Ø4-APR-76 16:56

HQM: NTFH15


;1A15
Y-7
Y-5
Y-3
Y-1
GND
Y-8
Y-6
Y-4
Y-2
Y-0
V12-MINUS
V-
DAC 100
RB
VCC
V12-PLUS
V+
V12-MINUS
SCALE
RS
Y-BACK
Y-OUT
;1A13
X-7
X-5
X-3
X-1
GND
X-8
X-6
X-4
X-2
X-0
V12-MINUS
V-
DAC 100
RB
VCC
V12-PLUS
V+
V12-MINUS
SCALE
RS
X-BACK
X-OUT
; Y-OUT AND X-OUT NEED PROTECTION DIODES
;1A9
; THIS IS A 72747 OP-AMP
NC
Y-OUT
GND
NC
V12-MINUS
NC
GND
1A08
NC
NC
V12-PLUS
Y-BACK
NC
V12-PLUS
NC
Y-SCOPE
X-OUT
X-OUT
Y-OUT
Y-OUT
1A09
GND
GND
GND
GND
;1 - 914 DIODE - 16
;2 - 914 DIODE - 15
;1K RES
;560 RES-160PF CAP
;3.8K RES-160PF CAP
;10K RES
;7 - 914 DIODE - 10
;8- 914 DIODE - 9
NC
X-OUT
GND
NC
V12-MINUS
NC
GND
1A10
NC
NC
V12-PLUS
X-BACK
NC
X-SCOPE
V12-PLUS
NC
;1A8
; ANALOG FEEDBACK NET
;PINS 4 AND 10 EACH HAVE 470PF CAP TO GND
;1A10
;PINS 9 10 15 16 HAVE DAC PROTECTION DIODES
; PUT NEAR VECTOR GENERATOR



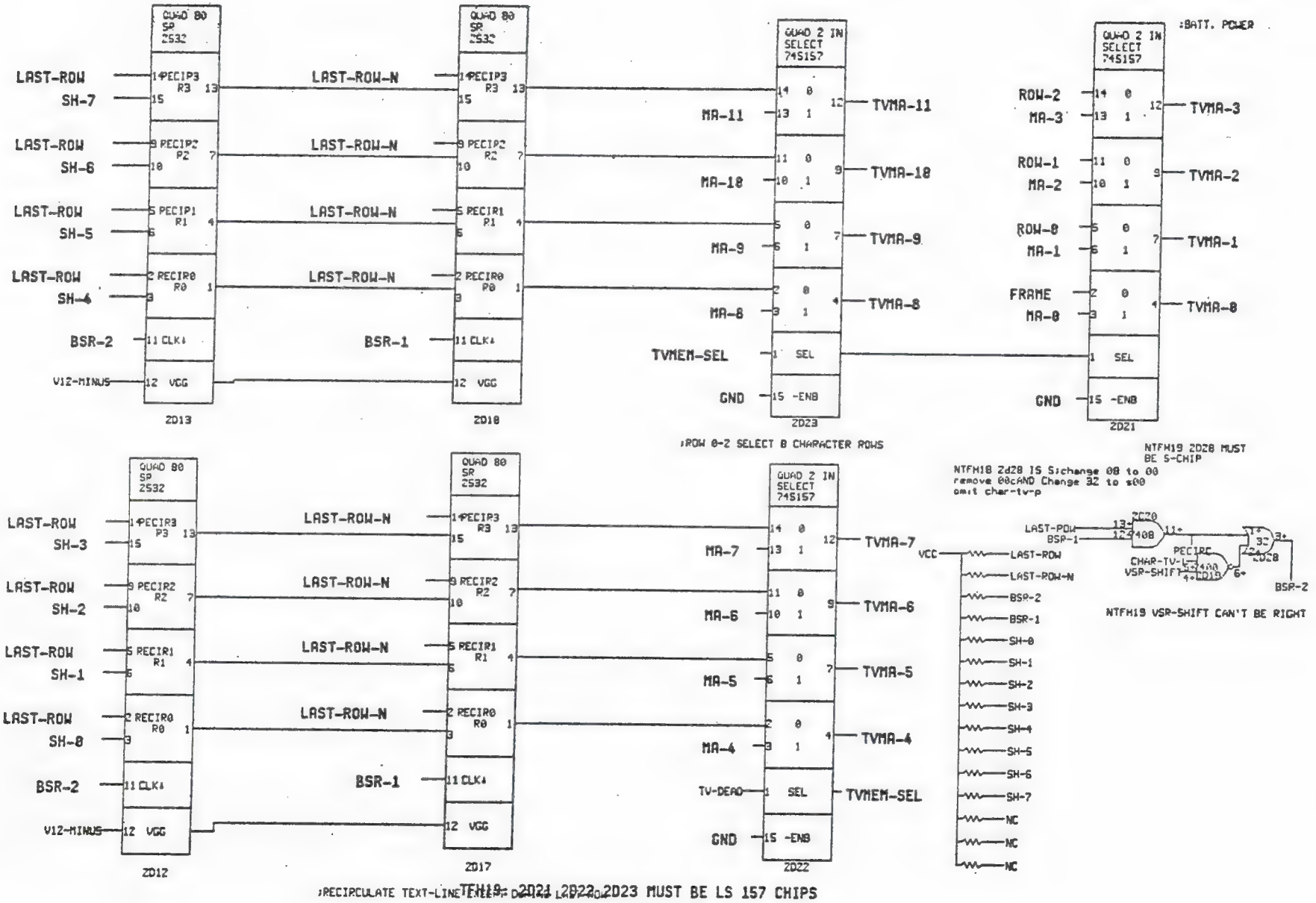
A-L-U CHIPS	MINSKY 2500	29-FEB-76 13:29	HQM: NTFH17

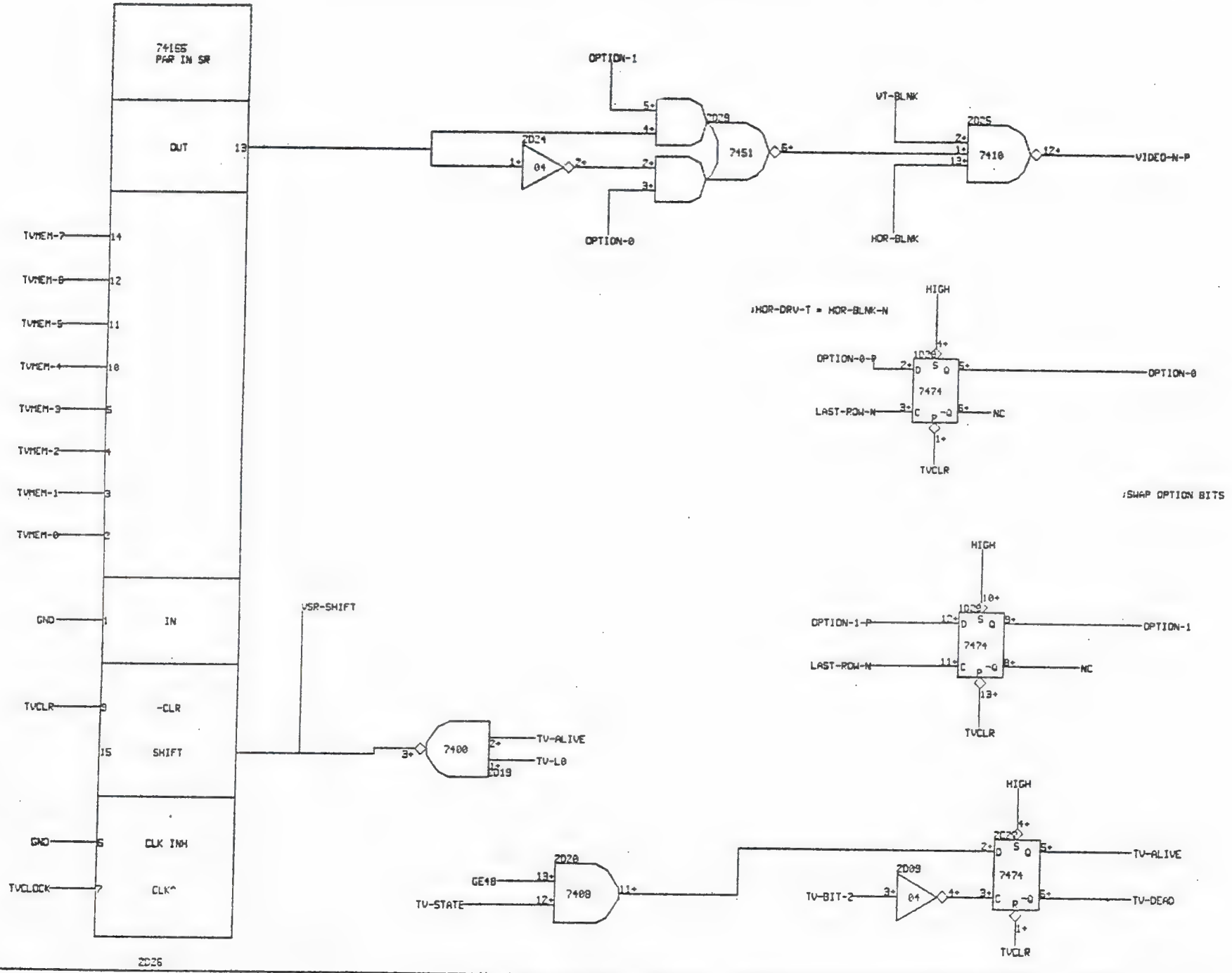


TIMING CHAIN

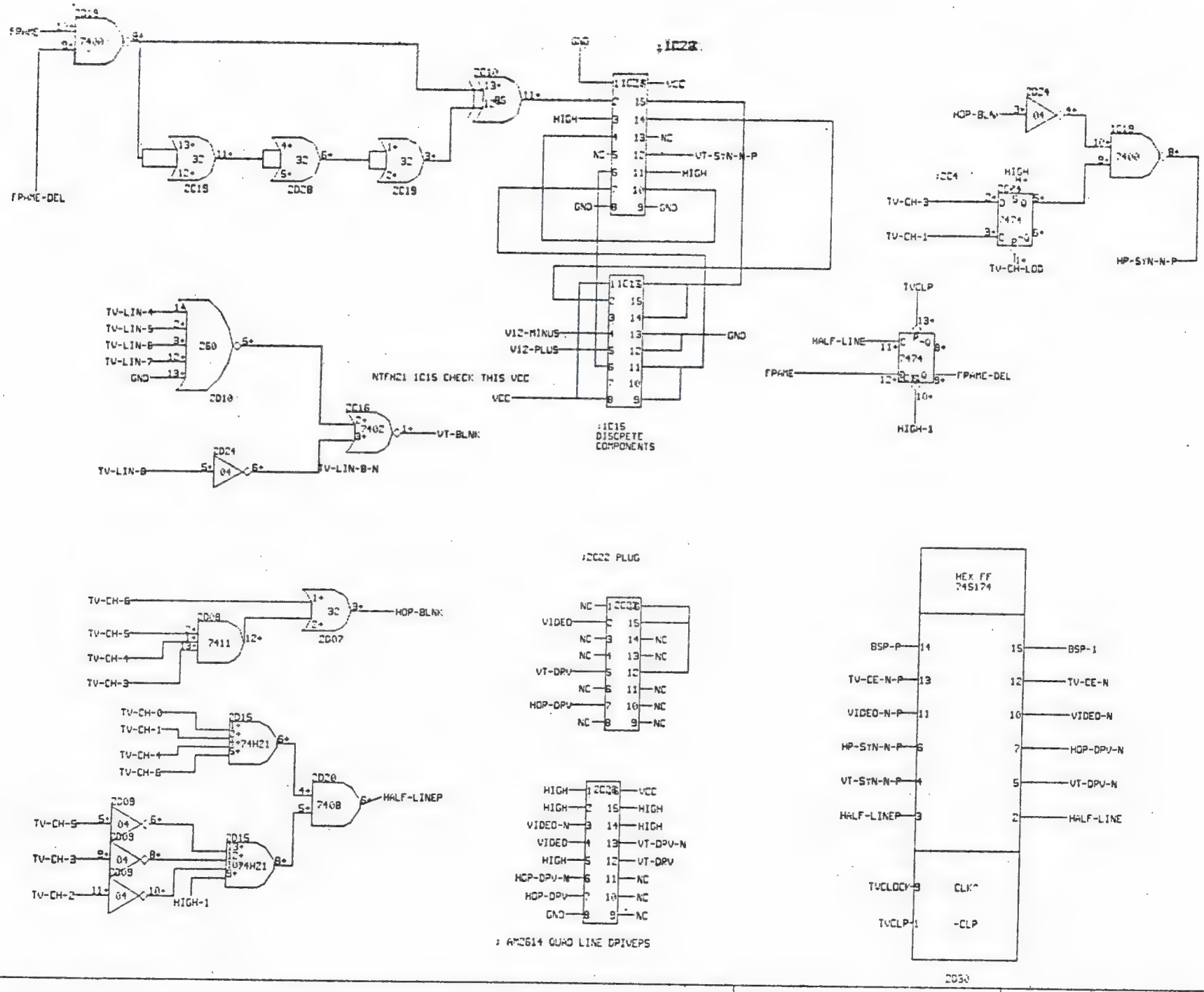
02-APR-76 15:14

HQM: NTFH18

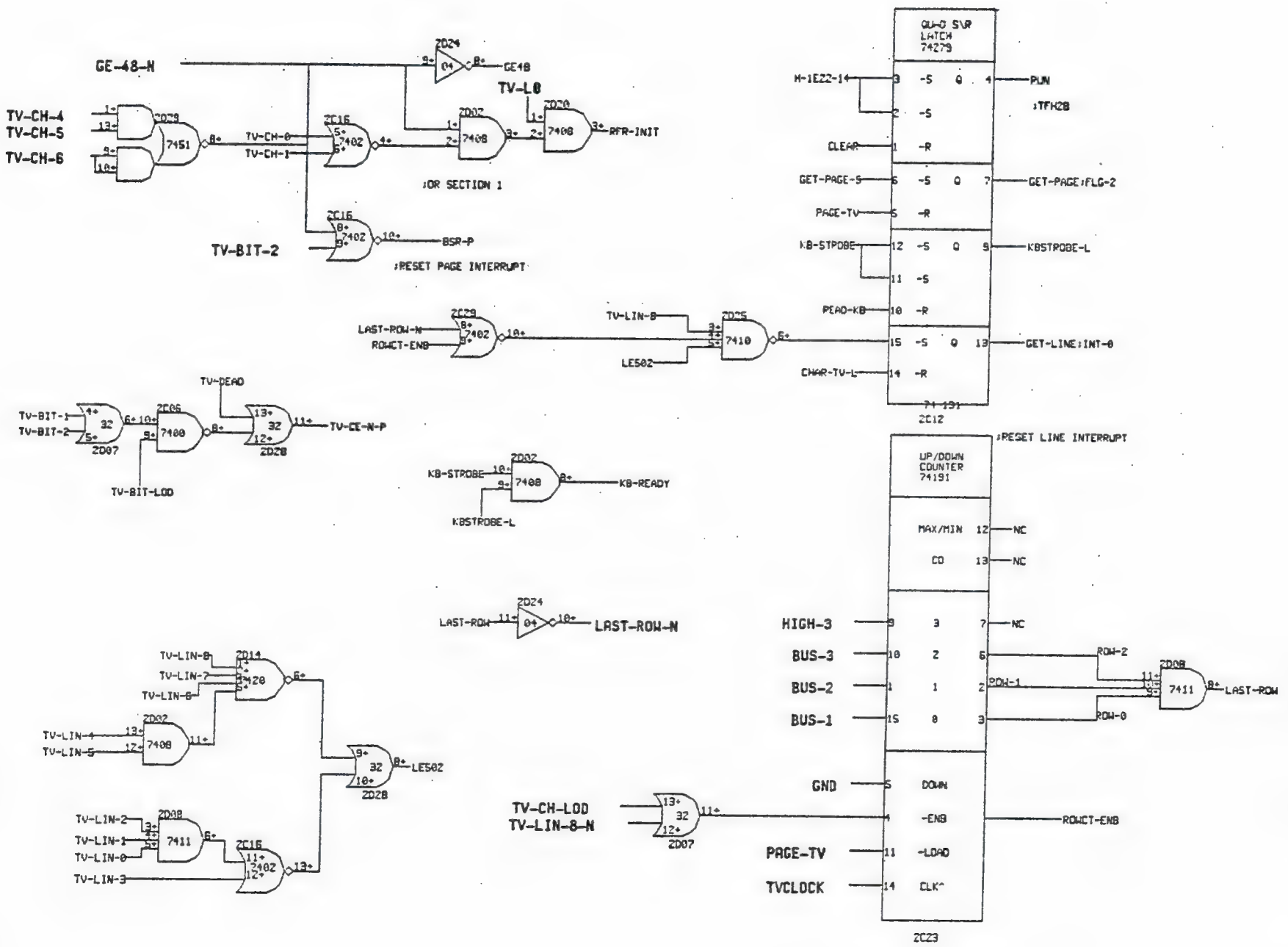

QUAD 80 SR 2532
ZD13
ZD18
QUAD 2 IN SELECT 74S157
ZD23
ZD21
ZD12
ZD17
ZD22
LAST-ROW
SH-7
SH-6
SH-5
SH-4
SH-3
SH-2
SH-1
SH-0
BSR-2
BSR-1
V12-MINUS
LAST-ROW-N
MA-11
MA-10
MA-9
MA-8
MA-7
MA-6
MA-5
MA-4
TVMEM-SEL
GND
TV-DEAD
TVMA-11
TVMA-10
TVMA-9
TVMA-8
TVMA-7
TVMA-6
TVMA-5
TVMA-4
TVMA-3
TVMA-2
TVMA-1
TVMA-0
ROW-2
ROW-1
ROW-0
FRAME
:BATT. POWER
:ROW 0-2 SELECT 8 CHARACTER ROWS
NTFH19 2D28 MUST BE 5-CHIP
NTFH18 2d28 IS S:change 08 to 00
remove 00cAND Change 32 to s00
omit char-tv-p
LAST-POW
VCC
NC
NTFH19 VSR-SHIFT CAN'T BE RIGHT
:RECIRCULATE TEXT-LINE TEMPS
TEN19: 2021,2022,2023 MUST BE LS 157 CHIPS



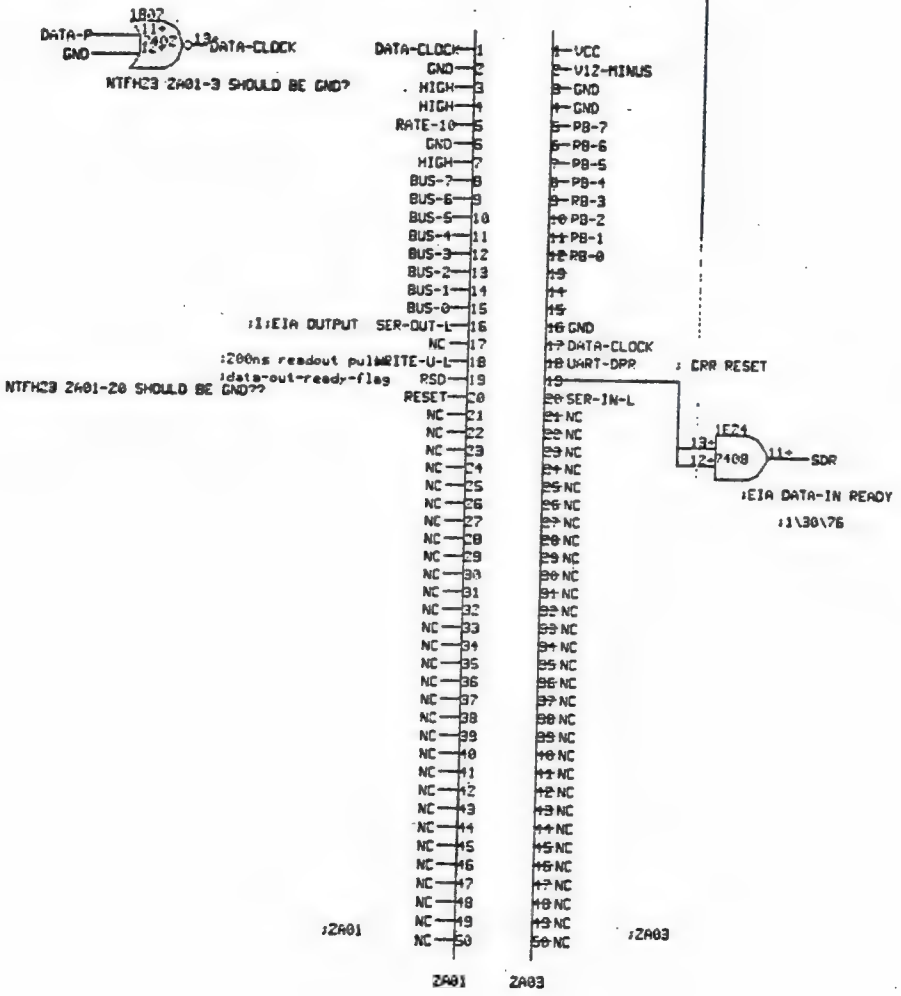
TV SIGNALS	INCLUDING DRIVERS	Ø2-APR-76 15:Ø9	HQM: NTFH2Ø



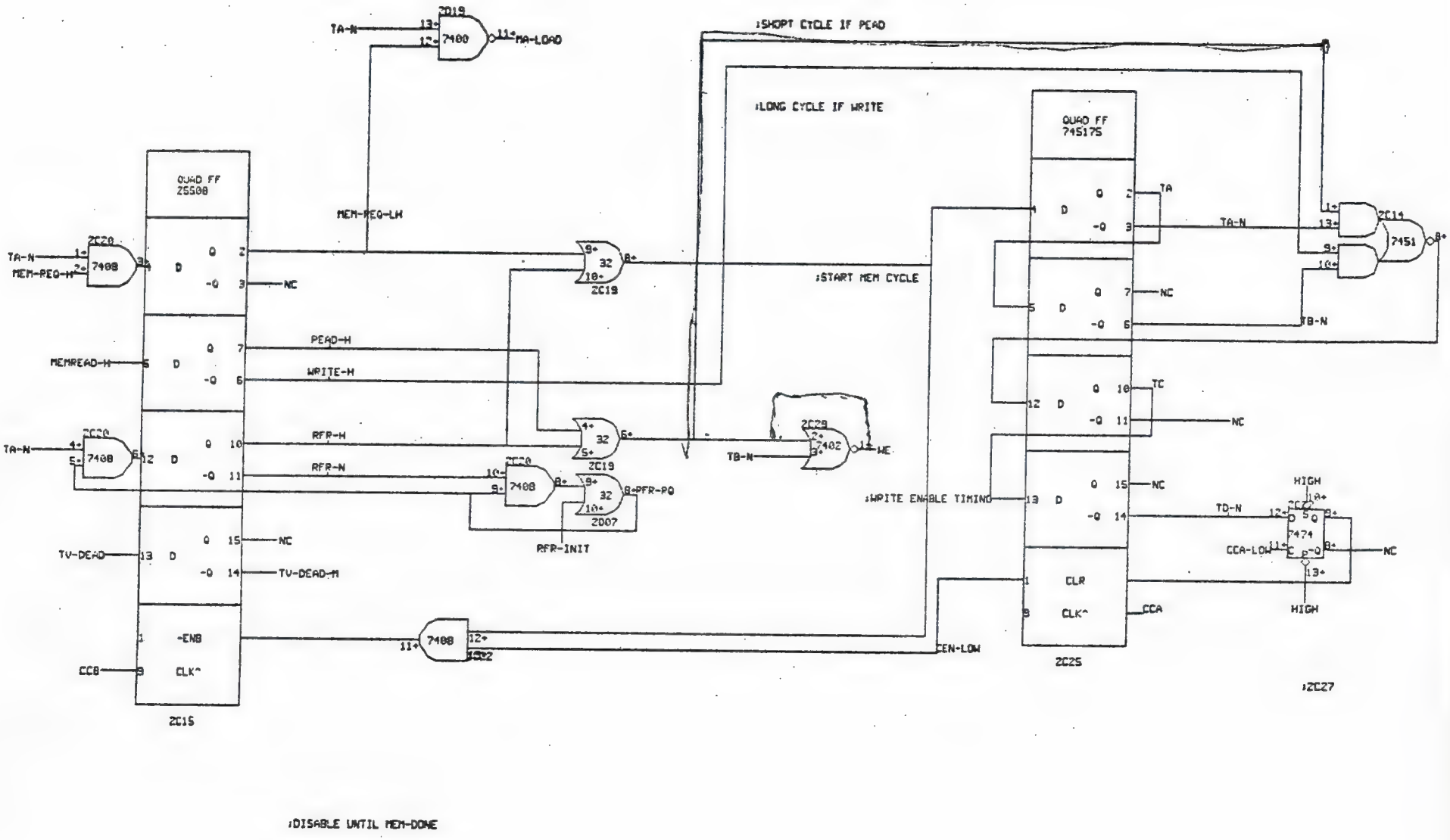
LINE BUFFERS | ADDRESS MULTIPLEXERS | Ø4-APR-76 22:18 | HQM: NTFH21



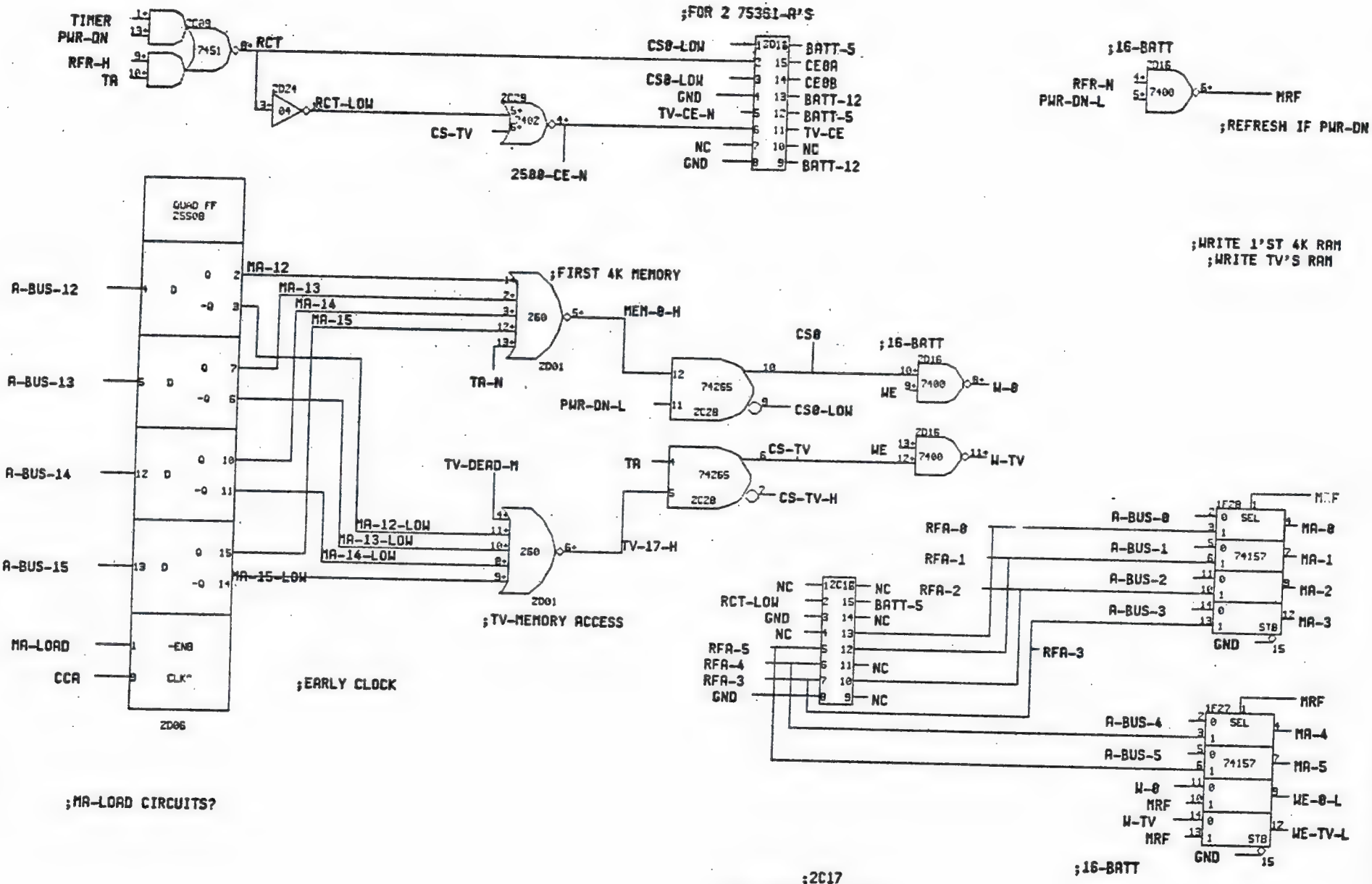
TV SIGNALS	INCLUDING DRIVERS	Ø2-APR-76 11:23	HQM: NTFH22



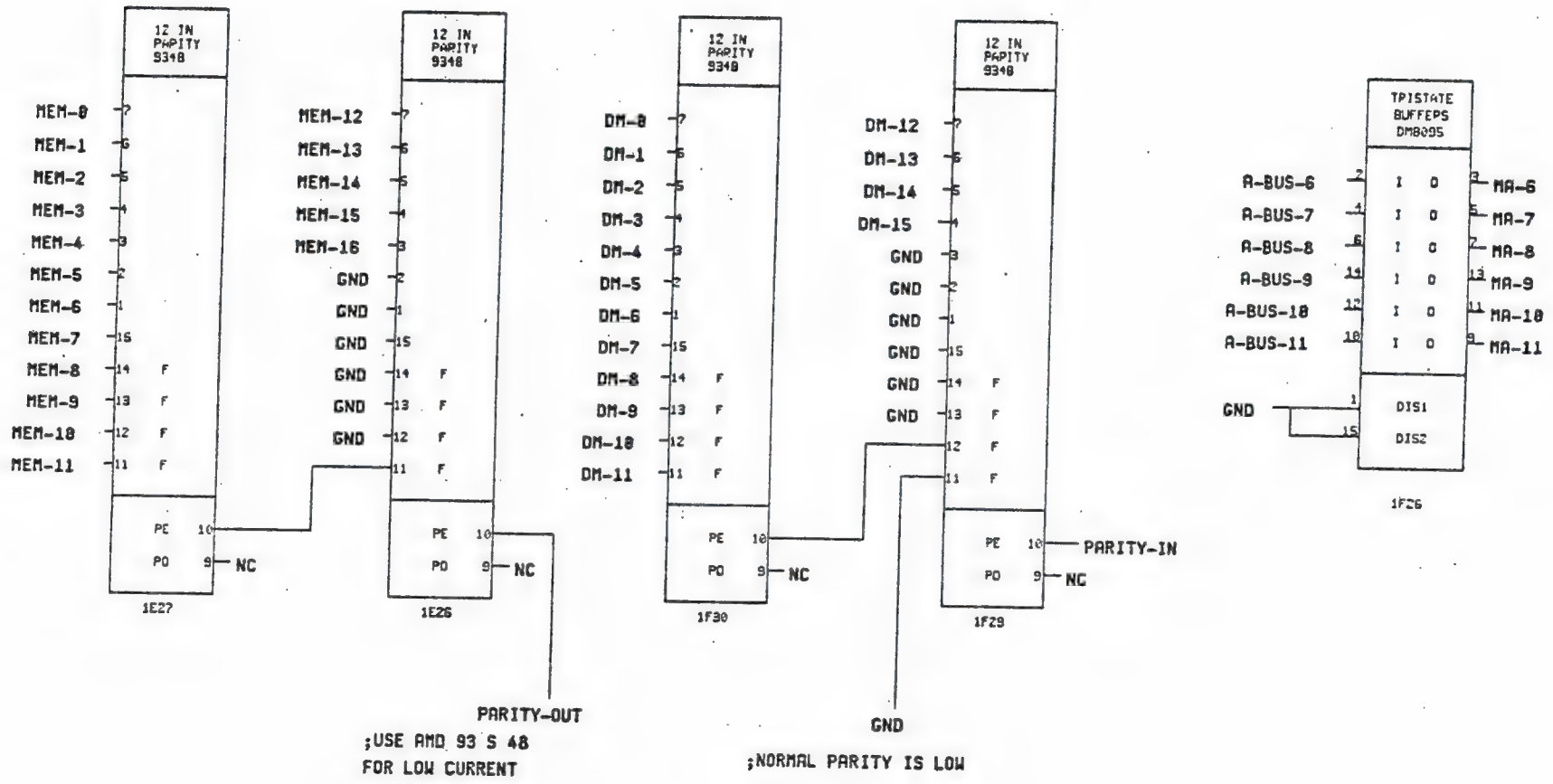
UART	UNIVERSAL SECTION	Ø2-APR-76 12:27	HQM: NTFH23

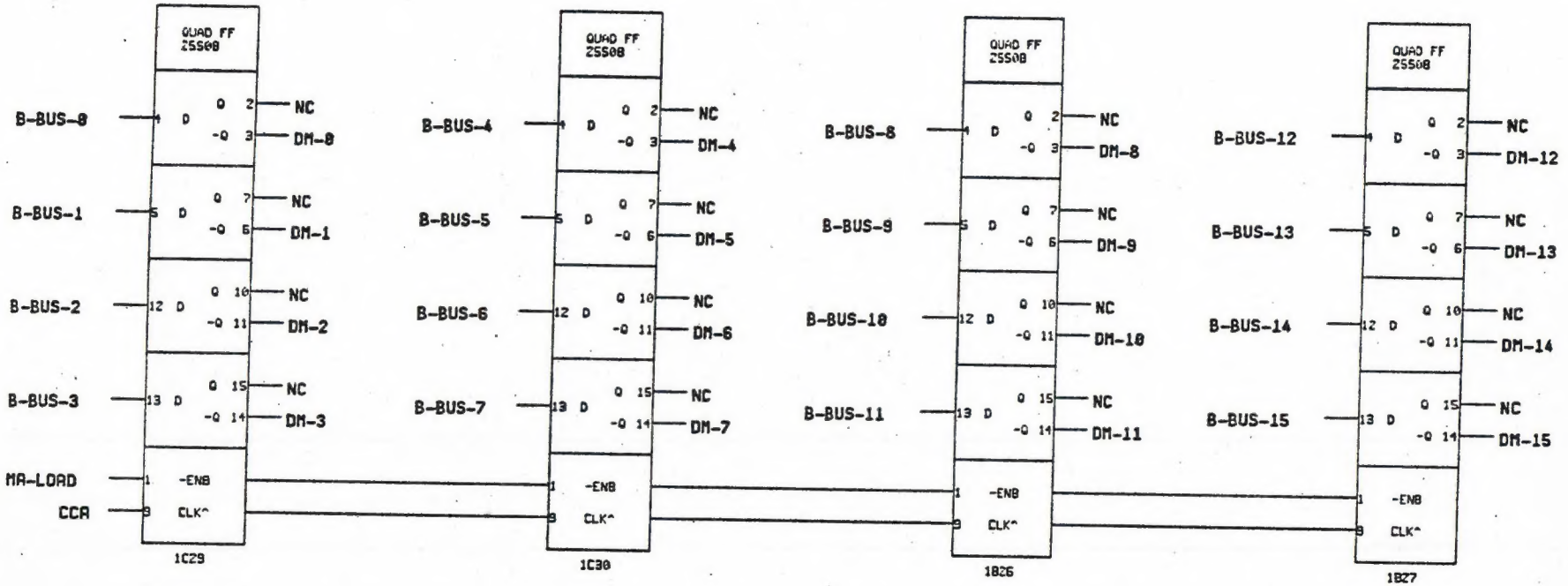


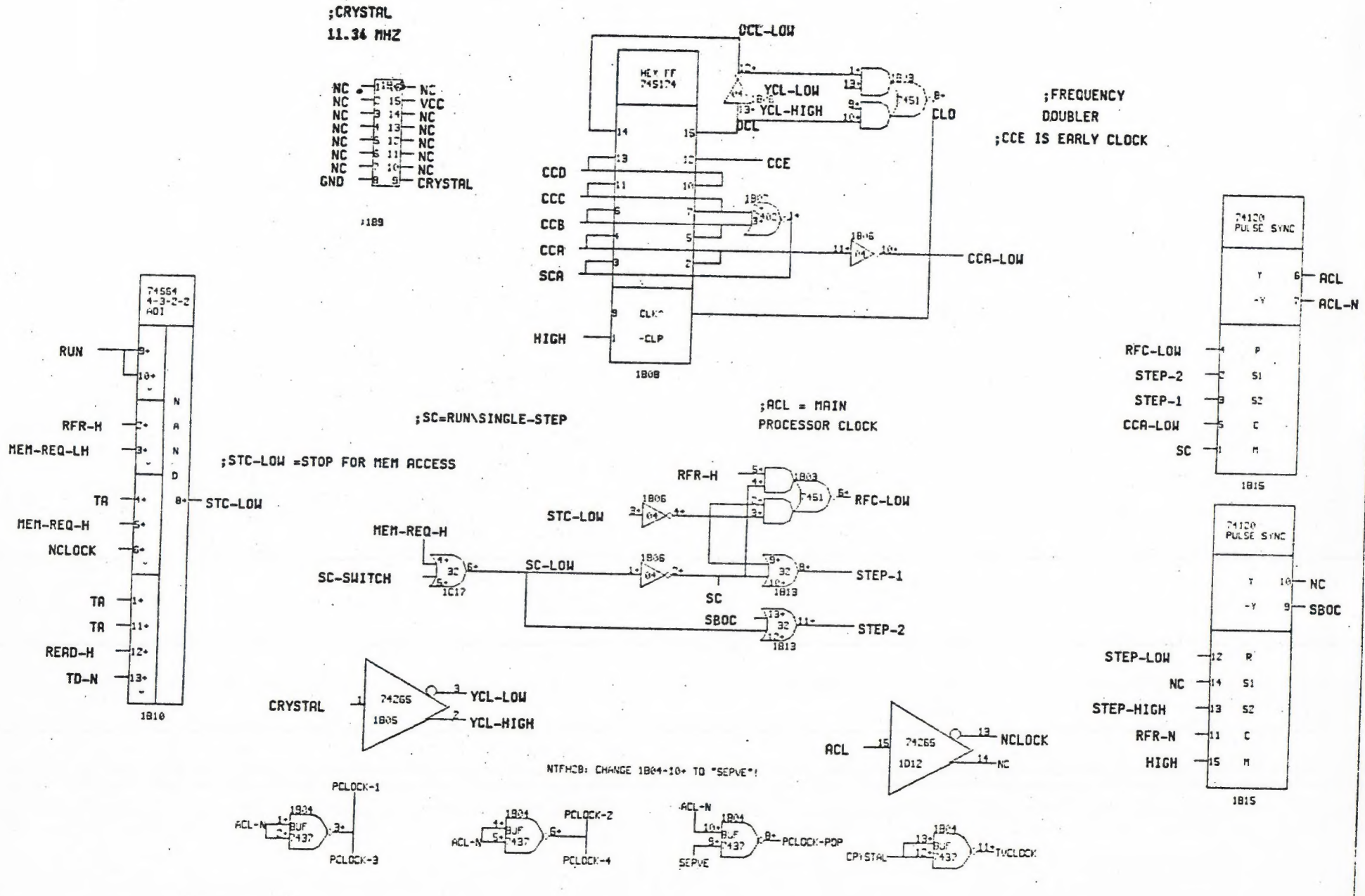
MEMORY CYCLE CONTROL	2500	29-FEB-76 14:17	HQM: NTFH24



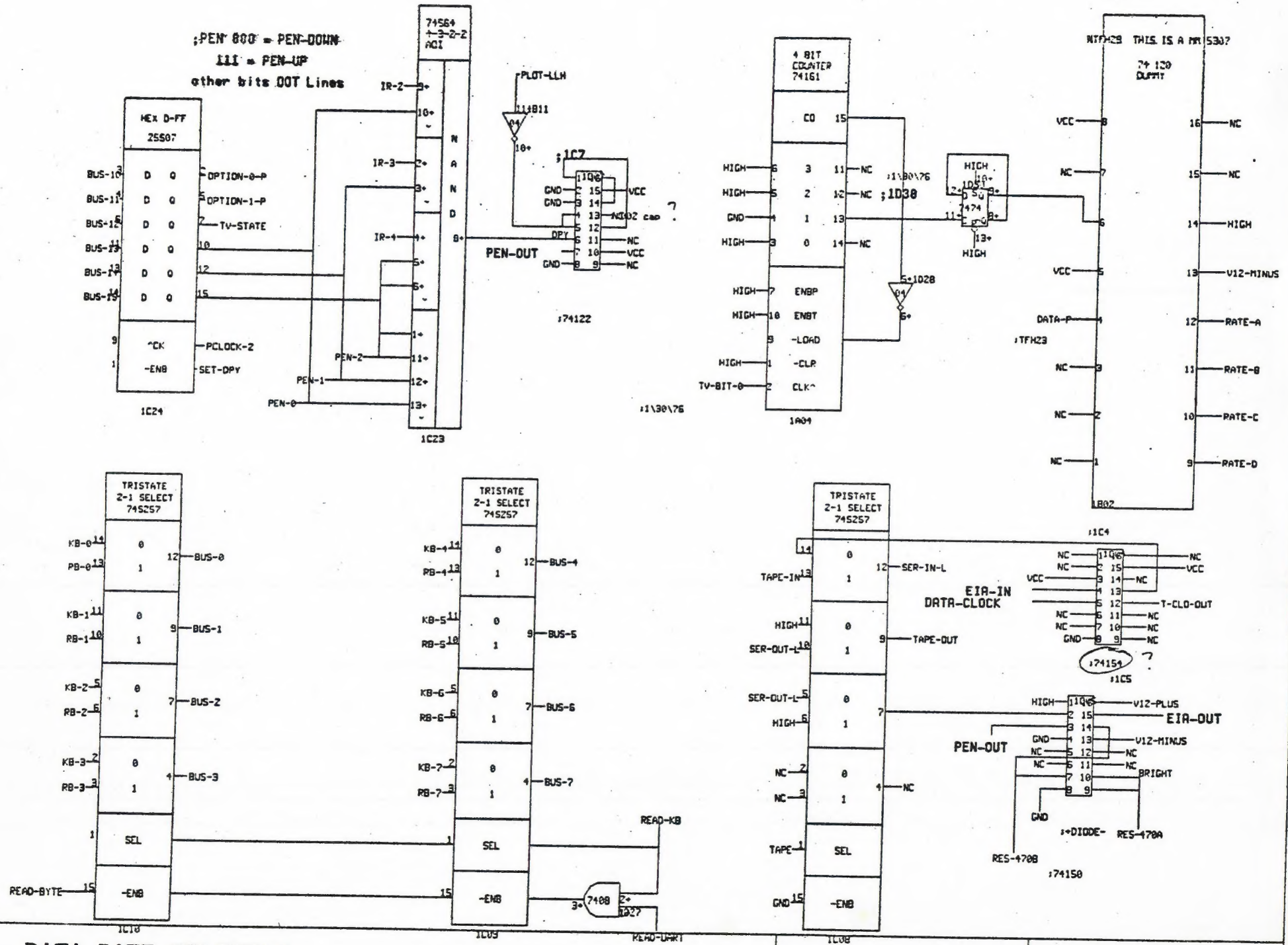
MEMORY ADDRESS REGISTER	2500	29-FEB-76 14:32	HQM: NTFH25


12 IN PARITY 9348
MEM-0
MEM-1
MEM-2
MEM-3
MEM-4
MEM-5
MEM-6
MEM-7
MEM-8
MEM-9
MEM-10
MEM-11
PE
PO
NC
1E27
MEM-12
MEM-13
MEM-14
MEM-15
MEM-16
GND
1E26
PARITY-OUT
;USE AMD 93 S 48
FOR LOW CURRENT
DM-0
DM-1
DM-2
DM-3
DM-4
DM-5
DM-6
DM-7
DM-8
DM-9
DM-10
DM-11
1F30
DM-12
DM-13
DM-14
DM-15
PARITY-IN
1F29
GND
;NORMAL PARITY IS LOW
TRISTATE BUFFERS DM8095
A-BUS-6
A-BUS-7
A-BUS-8
A-BUS-9
A-BUS-10
A-BUS-11
MA-6
MA-7
MA-8
MA-9
MA-10
MA-11
DIS1
DIS2
1F26


QUAD FF
25S08
B-BUS-0
B-BUS-1
B-BUS-2
B-BUS-3
MA-LOAD
CCA
NC
DM-0
DM-1
DM-2
DM-3
-ENB
CLK^
1C29
B-BUS-4
B-BUS-5
B-BUS-6
B-BUS-7
DM-4
DM-5
DM-6
DM-7
1C30
B-BUS-8
B-BUS-9
B-BUS-10
B-BUS-11
DM-8
DM-9
DM-10
DM-11
1B26
B-BUS-12
B-BUS-13
B-BUS-14
B-BUS-15
DM-12
DM-13
DM-14
DM-15
1B27



CLOCK CONTROL	2500	04-APR-76 22:57	HQM: NTFH28

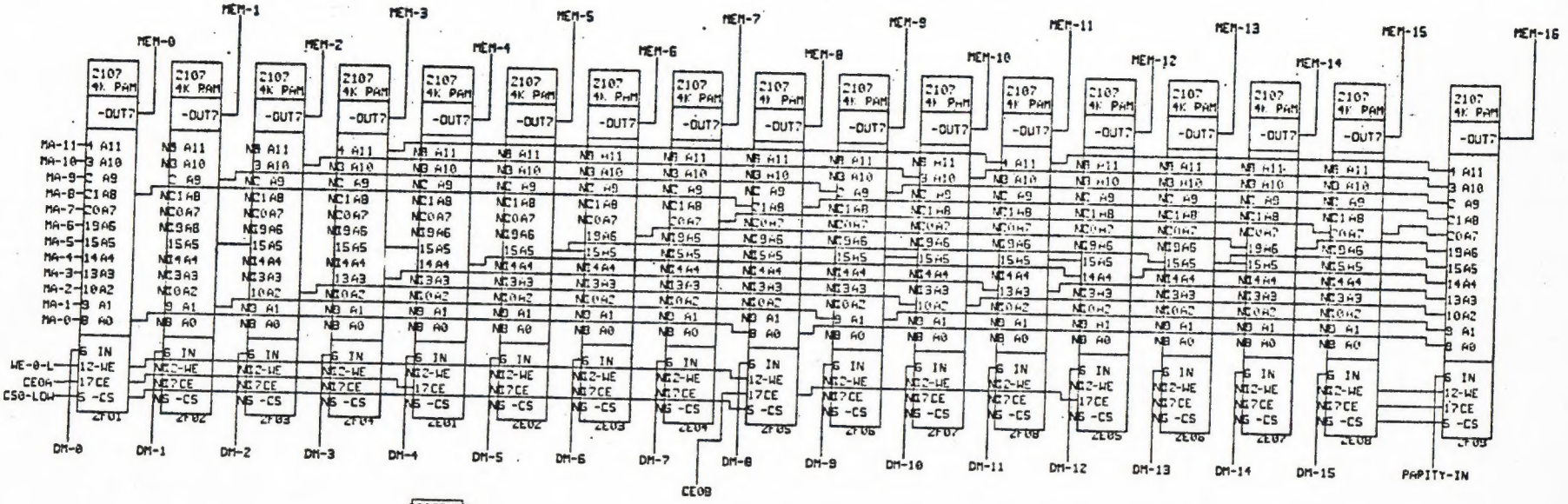


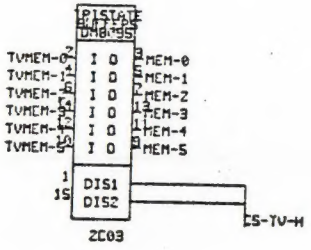
DATA RATE SELECTOR

31-MAR-76 16:27

HQM: NTFH29

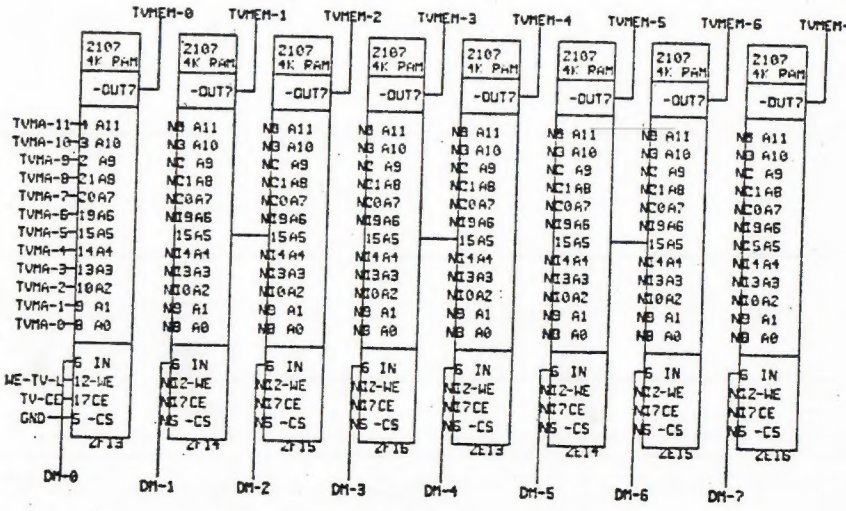
;FIRST 4K OF MAIN MEMORY on main board





;other two gates on
1C14 (TFH-10)

CONNECT
2E13-1 2EJ1-3 (BATT-5-N)
2E16-1 2EJ1-4
2E13-18 2EJ1-11 (BATT-12)
2E16-18 2EJ1-12
2E13-11 2EJ1-05 (BATT-5)
2E16-11 2EJ1-06
BE SURE WIRELIST DOESN'T CONNECT 1-18-11 ON MEMORY CHIPS



;use signetics 2604's

;4K BY 8-BIT FONT MEMORY